MT6323L PMIC Data Sheet

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Document Revision History

Revision	Date	Author	Description
1.0	2014/02/27	ShangYing Chung	Initial version
1.1	2014/04/08	ShangYing Chung	Revise ACCDET connection of audio block diagram in page.43
1.2	2015/06/22	ShangYing Chung	Revise package typo from 145L to 158L
1.3	2015/07/24	ShangYing Chung	Add RTC description and register table.

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1 Overview

1.1 Features

- Handles all MT8127 main chip power management
- Input range: 3.4 ~ 4.5V
- 3 buck converters and 24 LDOs optimized for specific tablet subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC and high-power/quality audio amplifier
- 32K RTC crystal oscillator for system timing, 1.8 and 2.8V clock buffer output
- Multiple function GPIO
- Flexibility for various configurations of indicator LED current source: 4ISINK
- SPI interface
- Li-ion battery charging function
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog timer
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- VFBGA - 158L package

1.2 Applications

Ideal for power management of MT8127 tablet and other portable systems.

1.3 General Descriptions

MT6323L is a power management system chip optimized for 2G/3G handsets and tablet, especially based on the MediaTek MT8117/MT8127 system solution. MT6323L contains 3 buck converters and 24 LDOs, which are optimized for specific tablet subsystems.

MT6323L provides mono 0.7W into 8Ω, high efficiency Class AB/D audio amplifiers and flexibility for various applications of indicator LED drivers. It supports up to 4 channel LEDs with independent controlled. Flexible control includes: register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6323L is optimized for maximum battery life. It allows the RTC circuit to stay alive without a battery for several hours. The battery charger in MT6323L supports lithium- ion (Li-ion) battery and provides pre-charge indication. The charger input voltage can be up to 10V and allows USB charging, too.

Some multi-purpose pins enable MT6323L to be configured in various applications.

MT6323L adopts SPI interface and SRCLKEN control pin to control buck converters, LDOs, Class AB/D, various drivers and charger. Besides, it provides enhanced safety control and protocol for handshaking with BB.

MT6323L is available in a VFBGA - 158L package. The operating temperature ranges from -25 to +85°C.

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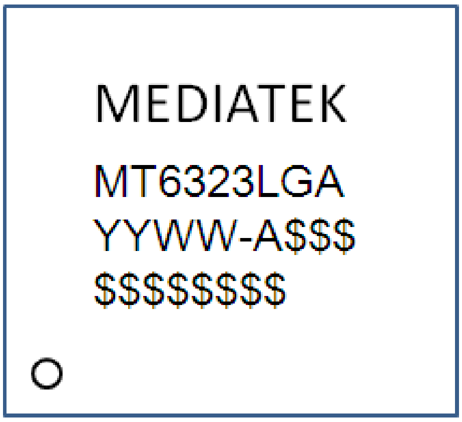
1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6323LGA/A		-25 ~ +85°C	VFBGA - 158L

1.5 Top Marking Definition

MT6323LGA/A



YYWW: Date Code

$: Random Code

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1.6 Pin Assignments and Descriptions

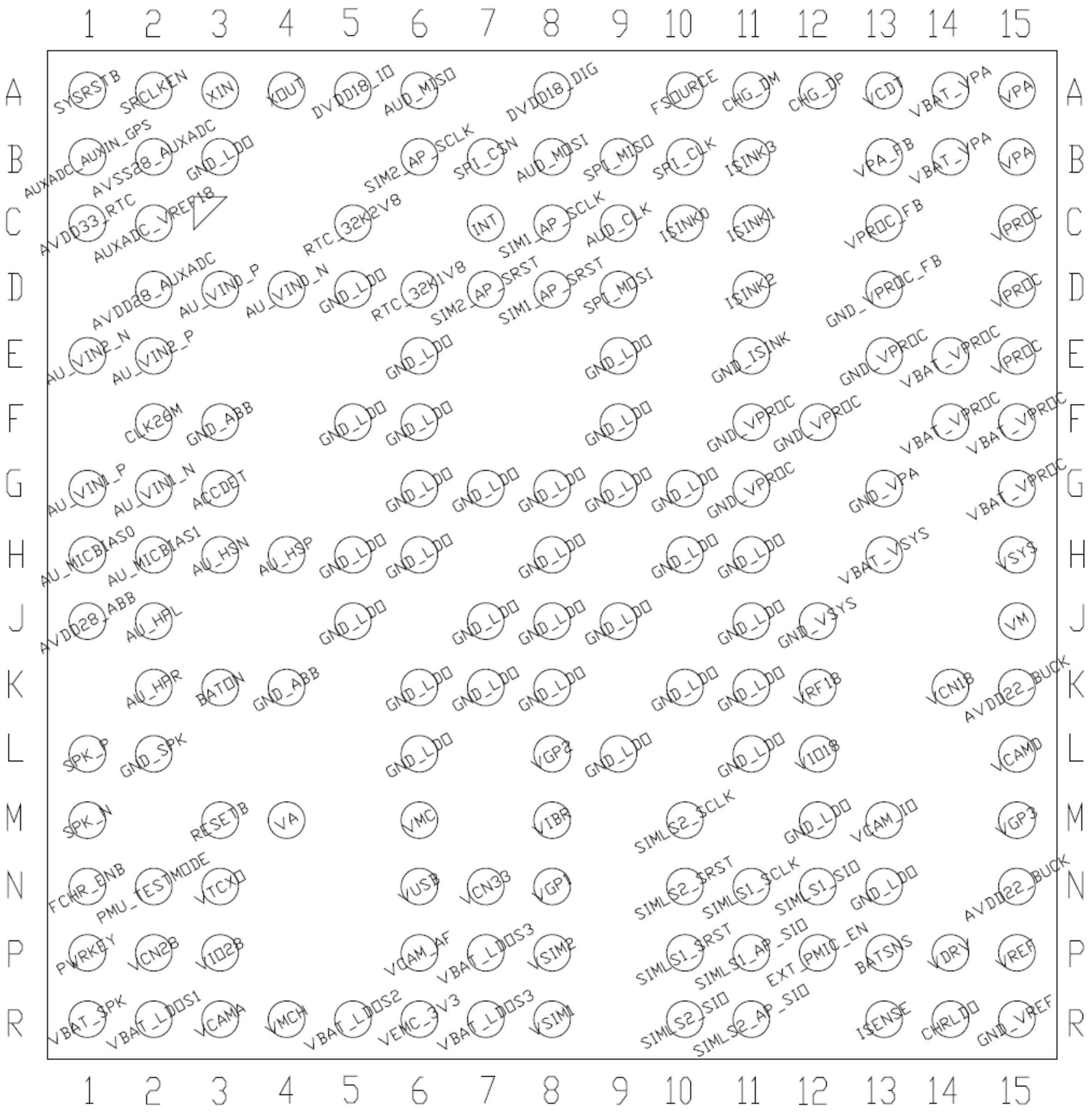

Figure 1-1. MT6323L VFBGA - 158L (7.6x7.6mm) pin assignment

Table 1-1. MT6323L pin descriptions

Ball	Symbol	I/O	Description
A1	SYSRSTB	I	Watchdog reset from AP
A10	FSOURCE	PWR	EFUSE power source
A11	CHG_DM	I	USB D- for BC1.1 standard
A12	CHG_DP	I	USB D+ for BC1.1 standard

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Ball	Symbol	I/O	Description
A13	VCDT	I	Fractional charger input voltage for charger detection
A14	VBAT_VPA	PWR	Battery power supply input of VPA
A15	VPA	O	SW node of VPA
A2	SRCLKEN	I	Enables 26MHz CLK
A3	XIN	I	1. One of 32K crystal connection port while using crystal to generate 32kHz clock 2. Tie to ground with 32kHz crystal absence
A4	XOUT	I	1. One of 32K crystal connection port while using crystal to generate 32kHz clock 2. External 32kHz clock input with 32kHz crystal absence
A5	DVDD18_IO	PWR	Power of VIO18 IO/CORE
A6	AUD_MISO	O	Uplink AUDIO ADC serial data
A8	DVDD18_DIG	PWR	Power of VDIG18
B1	AUXADC_AUXIN_GPS	I	AUXADC input
B10	SPI_CLK	I	SPI interface's clock
B11	ISINK3	O	Current sink channel 3 output
B13	VPA_FB	I	Feedback of VPA
B14	VBAT_VPA	PWR	Battery power supply input of VPA
B15	VPA	O	SW node of VPA
B2	AVSS28_AUXADC	GND	GND for AUXADC
B3	GND_LDO	GND	Ground for LDO
B6	SIM2_AP_SCLK	I	AP/PMIC SIM2 clock
B7	SPI_CSN	I	SPI interface's chip select signal to identify which device is selected
B8	AUD_MOSI	I	Downlink DAC serial data
B9	SPI_MISO	IO	SPI interface's serial data signal.Default: Output only.
C1	AVDD33_RTC	PWR	RTC LDO output. Supply of RTC macro where backup battery can be added.
C10	ISINK0	O	Current sink channel 0 output
C11	ISINK1	O	Current sink channel 1 output
C13	VPROC_FB	I	Feedback of VPROC
C15	VPROC	O	SW node of VPROC
C2	AUXADC_VREF18	O	1.8V AUXADC reference output
C5	RTC_32K2V8	O	RTC domain 32kHz clock output
C7	INT	O	Default: Output 0 Interrupt to BB, high active
C8	SIM1_AP_SCLK	I	AP/PMIC SIM1 clock

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Ball	Symbol	I/O	Description
C9	AUD_CLK	I	26M clock (can be hopping)
D11	ISINK2	O	Current sink channel 2 output
D13	GND_VPROC_FB	I	Remote sense on ground of VPROC
D15	VPROC	O	SW node of VPROC
D2	AVDD28_AUXADC	PWR	2.8V power input for AUXADC
D3	AU_VIN0_P	I	Analog input 1 positive
D4	AU_VIN0_N	I	Analog input 1 negative
D5	GND_LDO	GND	Ground for LDO
D6	RTC_32K1V8	O	VIO18 domain 32kHz clock output
D7	SIM2_AP_SRST	I	AP/PMIC SIM2 SRST
D8	SIM1_AP_SRST	I	AP/PMIC SIM1 SRST
D9	SPI_MOSI	IO	SPI interface's serial data signal. Default: Input only.
E1	AU_VIN2_N	I	Analog input 3 negative
E11	GND_ISINK	GND	GND for ISINK
E13	GND_VPROC	GND	Ground of VPROC
E14	VBAT_VPROC	PWR	Battery power supply input of VPROC
E15	VPROC	O	SW node of VPROC
E2	AU_VIN2_P	I	Analog input 3 positive
E6	GND_LDO	GND	Ground for LDO
E9	GND_LDO	GND	Ground for LDO
F11	GND_VPROC	GND	Ground of VPROC
F12	GND_VPROC	GND	Ground of VPROC
F14	VBAT_VPROC	PWR	Battery power supply input of VPROC
F15	VBAT_VPROC	PWR	Battery power supply input of VPROC
F2	CLK26M	I	26MHz CLK
F3	GND_ABB	GND	GND of ABB
F5	GND_LDO	GND	Ground for LDO
F6	GND_LDO	GND	Ground for LDO
F9	GND_LDO	GND	Ground for LDO
G1	AU_VIN1_P	I	Analog input 2 positive
G10	GND_LDO	GND	Ground for LDO
G11	GND_VPROC	GND	Ground of VPROC
G13	GND_VPA	GND	Ground of VPA
G15	VBAT_VPROC	PWR	Battery power supply input of VPROC
G2	AU_VIN1_N	I	Analog input 2 negative
G3	ACCDET	I	Accessory detection input
G6	GND_LDO	GND	Ground for LDO

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Ball	Symbol	I/O	Description
G7	GND_LDO	GND	Ground for LDO
G8	GND_LDO	GND	Ground for LDO
G9	GND_LDO	GND	Ground for LDO
H1	AU_MICBIAS0	PWR	Microphone bias for main and 2nd microphone
H10	GND_LDO	GND	Ground for LDO
H11	GND_LDO	GND	Ground for LDO
H13	VBAT_VSYS	PWR	Battery power supply input of VSYS BUCK
H15	VSYS	O	SW node of VSYS BUCK
H2	AU_MICBIAS1	PWR	Microphone bias for earphone
H3	AU_HSN	O	Receiver output
H4	AU_HSP	O	Receiver output
H5	GND_LDO	GND	Ground for LDO
H6	GND_LDO	GND	Ground for LDO
H8	GND_LDO	GND	Ground for LDO
J1	AVDD28_ABB	PWR	2.8V power input for ABB
J11	GND_LDO	GND	Ground for LDO
J12	GND_VSYS	GND	Ground of VSYS BUCK
J15	VM	O	VM output voltage
J2	AU_HPL	O	Headphone L-ch output
J5	GND_LDO	GND	Ground for LDO
J7	GND_LDO	GND	Ground for LDO
J8	GND_LDO	GND	Ground for LDO
J9	GND_LDO	GND	Ground for LDO
K10	GND_LDO	GND	Ground for LDO
K11	GND_LDO	GND	Ground for LDO
K12	VRF18	O	VRF18 output voltage
K14	VCN18	O	VCN18 output voltage
K15	AVDD22_BUCK	PWR	Power supply input of VSYSLDO
K2	AU_HPR	O	Headphone R-ch output
K3	BATON	I	Battery NTC pin for battery and its temperature sensing
K4	GND_ABB	GND	GND of ABB
K6	GND_LDO	GND	Ground for LDO
K7	GND_LDO	GND	Ground for LDO
K8	GND_LDO	GND	Ground for LDO
L1	SPK_P	O	Positive output for internal speaker amp
L11	GND_LDO	GND	Ground for LDO
L12	VIO18	O	VIO18 output voltage

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Ball	Symbol	I/O	Description
L15	VCAMD	O	VCAMD output voltage
L2	GND_SPK	GND	Ground for VBAT_SPK
L6	GND_LDO	GND	Ground for LDO
L8	VGP2	O	VGP2 output voltage
L9	GND_LDO	GND	Ground for LDO
M1	SPK_N	O	Negative output for Internal Speaker Amp
M10	SIMLS2_SCLK	O	SIMLS2 SCLK
M12	GND_LDO	GND	Ground for LDO
M13	VCAM_IO	O	VCAM_IO output voltage
M15	VGP3	O	VGP3 output voltage
M3	RESETB	O	System reset release signal
M4	VA	O	VA output voltage
M6	VMC	O	VMC output voltage
M8	VIBR	O	VIBR output voltage
N1	FCHR_ENB	I	Force charging ENB
N10	SIMLS2_SRST	O	SIMLS2 SRST
N11	SIMLS1_SCLK	O	SIMLS1 SCLK
N12	SIMLS1_SIO	IO	SIMLS1 data signal
N13	GND_LDO	GND	Ground for LDO
N15	AVDD22_BUCK	PWR	Power supply input of VSYSLDO
N2	PMU_TESTMODE	I	PMU testmode signal (tie to GND in normal operation)
N3	VTCXO	O	VTLDO output voltage
N6	VUSB	O	VSUB output voltage
N7	VCN33	O	VCN33 output voltage
N8	VGP1	O	VGP1 output voltage
P1	PWRKEY	I	Power key signal
P10	SIMLS1_SRST	O	SIMLS1 SRST
P11	SIMLS1_AP_SIO	IO	SIM1_AP data signal
P12	EXT_PMIC_EN	O	Enables external PMIC (VBAT domain)
P13	BATSNS	I	Negative terminal for battery's charging current sensing resistor
P14	VDRV	O	Charger current drive output
P15	VREF	O	Bandgap reference voltage
P2	VCN28	O	VCN28 output voltage
P3	VIO28	O	VIO28 output voltage
P6	VCAM_AF	O	VCAM_AF output voltage
P7	VBAT_LDOS3	PWR	LDO3 VBAT power

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Ball	Symbol	I/O	Description
P8	VSIM2	O	VSIM2 output voltage
R1	VBAT_SPK	PWR	Battery power supply input of SPK
R10	SIMLS2_SIO	IO	SIMLS2 data signal
R11	SIMLS2_AP_SIO	IO	SIM2_AP data signal
R13	ISENSE	I	Positive terminal for battery's charging current sensing resistor
R14	CHRLDO	O	Charger LDO28 output
R15	GND_VREF	GND	Ground for bandgap
R2	VBAT_LDOS1	PWR	LDO1 VBAT power
R3	VCAMA	O	VCAMA output voltage
R4	VMCH	O	VMCH output voltage
R5	VBAT_LDOS2	PWR	LDO2 VBAT power
R6	VEMC_3V3	O	VEMC_3V3 output voltage
R7	VBAT_LDOS3	PWR	LDO3 VBAT power
R8	VSIM1	O	VSIM1 output voltage

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed under Table 2-1. Absolute maximum ratings may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery input voltage range				4.5	V
ESD robustness	HBM	2,000			V
Charger input withstand				10	V

2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		39.15[1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

2.3 Recommended Operating Range

Table 2-2. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-25		65	°C

2.4 Electrical Characteristics

VBAT = 3.4 ~ 4.35V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

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Table 2-3. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation ground current					
Standby	Low-power mode		300		μA
Under voltage (UV)					
Under voltage falling threshold 1	UV_SEL[1:0] = 00	2.75	2.9	3.05	V
Under voltage falling threshold 2	UV_SEL[1:0] = 01		2.75		V
Under voltage falling threshold 3	UV_SEL[1:0] = 10		2.6		V
Under voltage falling threshold 4	UV_SEL[1:0] = 11		2.5		V
Under voltage rising threshold	UV_SEL[1:0] = xx	3.05	3.2	3.35	V
Reset generator					
Output high		V_{IO}-0.4			V
Output low				0.2	V
Output current (Ioh)	Vo > VIO-0.4V		1		mA
Delay Time from VTCXO turn on to RESETB release		41	82	164	ms
Interrupt					
Output high		V_{IO}-0.4			V
Output low				0.2	V
PWRKEY input					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time		25	50	200	ms
Control input voltage					
Control input high (HOMEKEY, SPI, SRCLKEN related)		0.7*VIO			V
Control input low (HOMEKEY, SPI, SRCLKEN related)				0.3*VIO	V
Thermal shut-down					
PMIC shut-down threshold			150		degree
SW high power latch threshold			125		degree
Interrupt threshold			105		degree

2.5 Regulator Output

Table 2-4. Regulator specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck - VPROC					
Output voltage			1.15		V
Output current			2,800		mA

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Parameter	Conditions	Min.	Typical	Max.	Unit
Load transient		-4		4	%
Load regulation		-1		1	%
Buck - VSYS					
Output voltage			2.2		V
Output current			1,400		mA
Load transient		-10		10	%
Buck – VPA					
Output voltage		0.5		3.4	V
Output current	VOUT = 3.4V		600		mA
Turn-on overshoot				10	%
ALDO - VA					
Output voltage			2.8		V
Output current			150		mA
Output noise	Freq = 10Hz to 80kHz Iout = 0.05Imax ~ full load		90		uVrms
PSRR	100Hz < freq < 3kHz Iout = 0.05Imax /0.5Imax		65		dB
	3kHz < freq < 30kHz Iout = 0.05Imax /0.5Imax		45		
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
ALDO – VTCXO					
Output voltage			2.8		V
Output current			40		mA
Output noise	Freq = 10Hz to 80kHz Iout = 0.05Imax ~ full load		90		uVrms
PSRR	100Hz < freq < 3kHz Iout = 0.05Imax /0.5Imax		40		dB
	3kHz < freq < 30kHz Iout = 0.05Imax /0.5Imax		25		
Turn-on rise time	No load		100		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
ALDO – VCN28					

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Parameter	Conditions	Min.	Typical	Max.	Unit
Output voltage	RF application		2.8		V
Output current			30		mA
Output noise	Freq = 10Hz to 80kHz Iout = 0.1Imax ~ full load		90		uVrms
PSRR	100Hz < freq < 3kHz Iout = 0.1Imax/0.5Imax		65		dB
	3kHz < freq < 30kHz Iout = 0.1Imax/0.5Imax		45		
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
ALDO – VCAMA					
Output voltage			2.8		V
Output current			150		mA
Output noise	Freq = 10Hz to 80kHz Iout = 0.01Imax ~ full load		40		uVrms
PSRR	100Hz < freq < 3kHz Iout = 0.01Imax/0.5Imax		65		dB
	3kHz < freq < 30kHz Iout = 0.01Imax/0.5Imax		45		
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-3		+3	%
Line/Load regulation		-3		+3	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VCN33					
Output voltage	VCAMA_SEL = 00		3.3		V
	VCAMA_SEL = 01		3.4		V
	VCAMA_SEL = 10		3.5		V
	VCAMA_SEL = 11		3.6		V
Output current			350		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%

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Parameter	Conditions	Min.	Typical	Max.	Unit
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VIO28					
Output voltage			2.8		V
Output current			200		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – USB					
Output voltage			3.3		V
Output current			20		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VMC					
Output voltage	VMC_SEL = 0		1.8		V
	VMC_SEL = 1		3.3		V
Output current			100		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load		40		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA

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Parameter	Conditions	Min.	Typical	Max.	Unit
DLDO – VMCH					
Output voltage	VMCH_SEL = 0		3.0		V
	VMCH_SEL = 1		3.3		V
Output current			400		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		40		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VEMC_3V3					
Output voltage	VEMC_3V3_SEL = 0		3.0		V
	VEMC_3V3_SEL = 1		3.3		V
Output current			400		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		40		us
Load transient response	IOUT = 0.1mA to 50mA (100mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VCAM_AF					
Output voltage	VEMC_1V8_SEL = 000		1.2		V
	VEMC_1V8_SEL = 001		1.3		V
	VEMC_1V8_SEL = 010		1.5		V
	VEMC_1V8_SEL = 011		1.8		V
	VEMC_1V8_SEL = 100		2.0		V
	VEMC_1V8_SEL = 101		2.8		V
	VEMC_1V8_SEL = 110		3		V
	VEMC_1V8_SEL = 111		3.3		V
Output current			100		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load	-5		+5	%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	(15mA/usec)				
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VGP1					
Output voltage	VGP1_SEL = 000		1.2		V
	VGP1_SEL = 001		1.3		V
	VGP1_SEL = 010		1.5		V
	VGP1_SEL = 011		1.8		V
	VGP1_SEL = 100		2.0		V
	VGP1_SEL = 101		2.8		V
	VGP1_SEL = 110		3		V
	VGP1_SEL = 111		3.3		V
Output current			100		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VGP2					
Output voltage	VGP2_SEL = 000		1.2		V
	VGP2_SEL = 001		1.3		V
	VGP2_SEL = 010		1.5		V
	VGP2_SEL = 011		1.8		V
	VGP2_SEL = 100		2.5		V
	VGP2_SEL = 101		2.8		V
	VGP2_SEL = 110		3.0		V
	VGP2_SEL = 111		2.0		V
Output current			100		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	

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Parameter	Conditions	Min.	Typical	Max.	Unit
Low power mode quiescent current			15		uA
DLDO – VSIM1					
Output voltage	VSIM1_SEL = 000		1.8		V
	VSIM1_SEL = 001		3.0		V
Output current			50		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-4		+4	%
Line/Load regulation		-4		+4	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VSIM2					
Output voltage	VSIM2_SEL = 000		1.8		V
	VSIM2_SEL = 001		3.0		V
Output current			50		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-4		+4	%
Line/Load regulation		-4		+4	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
DLDO – VIBR					
Output voltage	VIBR_SEL = 000		1.2		V
	VIBR_SEL = 001		1.3		V
	VIBR_SEL = 010		1.5		V
	VIBR_SEL = 011		1.8		V
	VIBR_SEL = 100		2.0		V
	VIBR_SEL = 101		2.8		V
	VIBR_SEL = 110		3.0		V
	VIBR_SEL = 111		3.3		V
Output current			100		mA
Dropout voltage			350		mV
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load	-5		+5	%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	(15mA/usec)				
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
VSYS LDO – VM					
Output voltage	VM_SEL = 00		1.24		V
	VM_SEL = 01		1.35		V
	VM_SEL = 10		1.5		V
	VM_SEL = 11		1.84		V
Output current			700		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (50mA/usec)	-3		+3	%
Line/Load regulation		-3		+3	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
VSYS LDO – VRF18					
Output voltage			1.825		V
Output current			200		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
VSYS LDO – VIO18					
Output voltage			1.8		V
Output current			300		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent			15		uA

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Parameter	Conditions	Min.	Typical	Max.	Unit
current					
VSYS LDO – VCN18					
Output voltage			1.8		V
Output current			120		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
VSYS LDO – VCAMD					
Output voltage	VCAMD_SEL = 00		1.2		V
	VCAMD _SEL = 01		1.3		V
	VCAMD _SEL = 10		1.5		V
	VCAMD _SEL = 11		1.8		V
Output current			150		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-3		+3	%
Line/Load regulation		-2.5		+2.5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
VSYS LDO – VCAM_IO					
Output voltage			1.8		V
Output current			100		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA
VSYS LDO – VGP3					
Output voltage			1.2		V

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Parameter	Conditions	Min.	Typical	Max.	Unit
			1.3		V
			1.5		V
			1.8		V
Output current			200		mA
PSRR	Freq = 217Hz Iout =0.05Imax /0.5Imax		40		dB
Turn-on rise time	No load		300		us
Load transient response	IOUT = 1mA to full load (15mA/usec)	-5		+5	%
Line/Load regulation		-5		+5	%
Short current		Imax*1.2		Imax*5	
Low power mode quiescent current			15		uA

2.6 Class AB/D Audio Amplifier

Table 2-5. Class AB/D audio amplifier specifications

Class AB parameter	Conditions	Min.	Typical	Max.	Unit
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		850		mW
	8Ω load, VBAT = 3.7V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		600		mW
THD+N	1kHz, Po = 0.5Wrms, 4.2V		0.05	0.2	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground		50		dB
Noise level	VBAT = 3.3V 0dB gain 8Ω, A-weighted			100	µV
	VBAT = 4.2V 0dB gain 8Ω, A-weighted			100	uV
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load		3	6	mA
CMRR	VBAT = 3.4/3.8/4.2V F = 1kHz, Vin = 200mVpk-	49	60		dB

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Class AB parameter	Conditions	Min.	Typical	Max.	Unit
	pk				

Class D parameter	Conditions	Min.	Typical	Max.	Unit
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		850		mW
	8Ω load, VBAT = 3.7V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		600		mW
THD+N	1kHz, Po = 0.5Wrms, 4.2V			0.2	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground		50		dB
Noise level	VBAT = 3.3V 0dB gain 8Ω, A-weighted			100	μV
	VBAT = 4.2V 0dB gain 8Ω, A-weighted			100	uV
Efficiency	VBAT = 4.2V 0.8W, 8Ω with 68uH, 1kHz	80	90		%
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load		4	6	mA
CMRR	VBAT = 3.4/3.8/4.2V F = 1kHz, Vin = 200mVpk-pk	49	60		dB

2.7 Battery Charger

Table 2-6. Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
CHRIN voltage		4.3	5	10.5	V
Operation range VCHRIN		3.2	5	7	V
OTG detection		0.8	2.4	4	V
VCDT CHRIN detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4.3		10.5	V
HV adaptive current @ pre_charge	CHRIN switch threshold (200mA => 70mA)		7		V

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Parameter	Conditions	Min.	Typical	Max.	Unit
	CHRIN switch threshold (70mA => 200mA)		6		V
VBAT CC		3.15	3.3	3.45	V
VBAT CV		4.15	4.2	4.25	V
VBAT OV		4.25	4.3	4.35	V
CC mode charging current	CS_VTH = 1111		$14/R_{sense}$		mA
	CS_VTH = 1110		$40/R_{sense}$		mA
	CS_VTH = 1101		$60/R_{sense}$		mA
	CS_VTH = 1100		$90/R_{sense}$		mA
	CS_VTH = 1011		$110/R_{sense}$		mA
	CS_VTH = 1010		$130/R_{sense}$		mA
	CS_VTH = 1001		$140/R_{sense}$		mA
	CS_VTH = 1000		$160/R_{sense}$		mA
	CS_VTH = 0111		$180/R_{sense}$		mA
	CS_VTH = 0110		$200/R_{sense}$		mA
	CS_VTH = 0101		$220/R_{sense}$		mA
	CS_VTH = 0100		$240/R_{sense}$		mA
	CS_VTH = 0011		$260/R_{sense}$		mA
	CS_VTH = 0010		$280/R_{sense}$		mA
	CS_VTH = 0001		$300/R_{sense}$		mA
	CS_VTH = 0000		$320/R_{sense}$		mA
UVLO	VTHH		3.2		V
	VTHL		2.75		V

2.8 Driver

Table 2-7. Driver specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
ISINK					
ISINK current matching	VISINK = 0.3 ~ 2.5V 4/24mA, 4 LEDs	-5		5	%
ISINK LED sink current (Normal Mode)	ISINK_SEL = 000		4		mA
	ISINK_SEL = 001		8		mA
	ISINK_SEL = 010		12		mA
	ISINK_SEL = 011		16		mA
	ISINK_SEL = 100		20		mA
	ISINK_SEL = 101		24		mA
ISINK LED sink current (Curret Double)	ISINK_SEL = 000		8		mA
	ISINK_SEL = 001		16		mA

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Parameter	Conditions	Min.	Typical	Max.	Unit
	ISINK_SEL = 010		24		mA
	ISINK_SEL = 011		32		mA
	ISINK_SEL = 100		40		mA
	ISINK_SEL = 101		48		mA
ISINK dropout voltage (Normal Mode)	4 ~ 24mA VISINK drop		150		mV
ISINK dropout voltage (Current Double)	8 ~ 48mA VISINK drop		250		mV
ISINK rise/fall time	VISINK > 0.3V			3.33	uS

2.9 BC1.1

Parameter	Conditions	Min.	Typical	Max.	Unit
BC11 charging port detection (Pre-CC current)	Standard down-stream port	35	70	94	mA
	Standard charging down-stream port	35	70	94	mA
	DP, DM short	140	200	260	mA
	DP, DM floating	140	200	260	mA
BC11 characteristics	IPU_DP, IPU_DM		9.6		uA
	IPD_DP, IPD_DM		96		uA
	VSRC on DP, DM		630		mV
	Current pulse value under 2.2V		70		mA
	Current pulse period under 2.2V		550		ms
	OSC1M, timer		5		min
	OSC1M, timer		35		min

2.10 Down Load Without Battery

Parameter	Conditions	Min.	Typical	Max.	Unit
USBDL	Duration		32.0		s
	Current		550		mA

2.11 AUXADC

Symbol	Parameter	Min.	Typical	Max.	Unit
N	Resolution		15		Bit
FC	Data rate		1		kHz
CIN	Input capacitance				

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Symbol	Parameter	Min.	Typical	Max.	Unit
	Unselected channel Selected channel			50 1	fF pF
RIN	Input resistance Unselected channel Selected channel	 400 1			 MΩ MΩ
SNR	Signal to noise ratio		85		dB
T	Operating temperature	-20		80	°C
Iq	Current consumption Power-up Power-down			 2 1	 mA μA

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3 Functional Descriptions

3.1 General Descriptions

MT6323L is a fully integrated PMIC target for tablet power provider. See Figure 3-1. the block diagram for the whole picture of MT6323L PMIC.

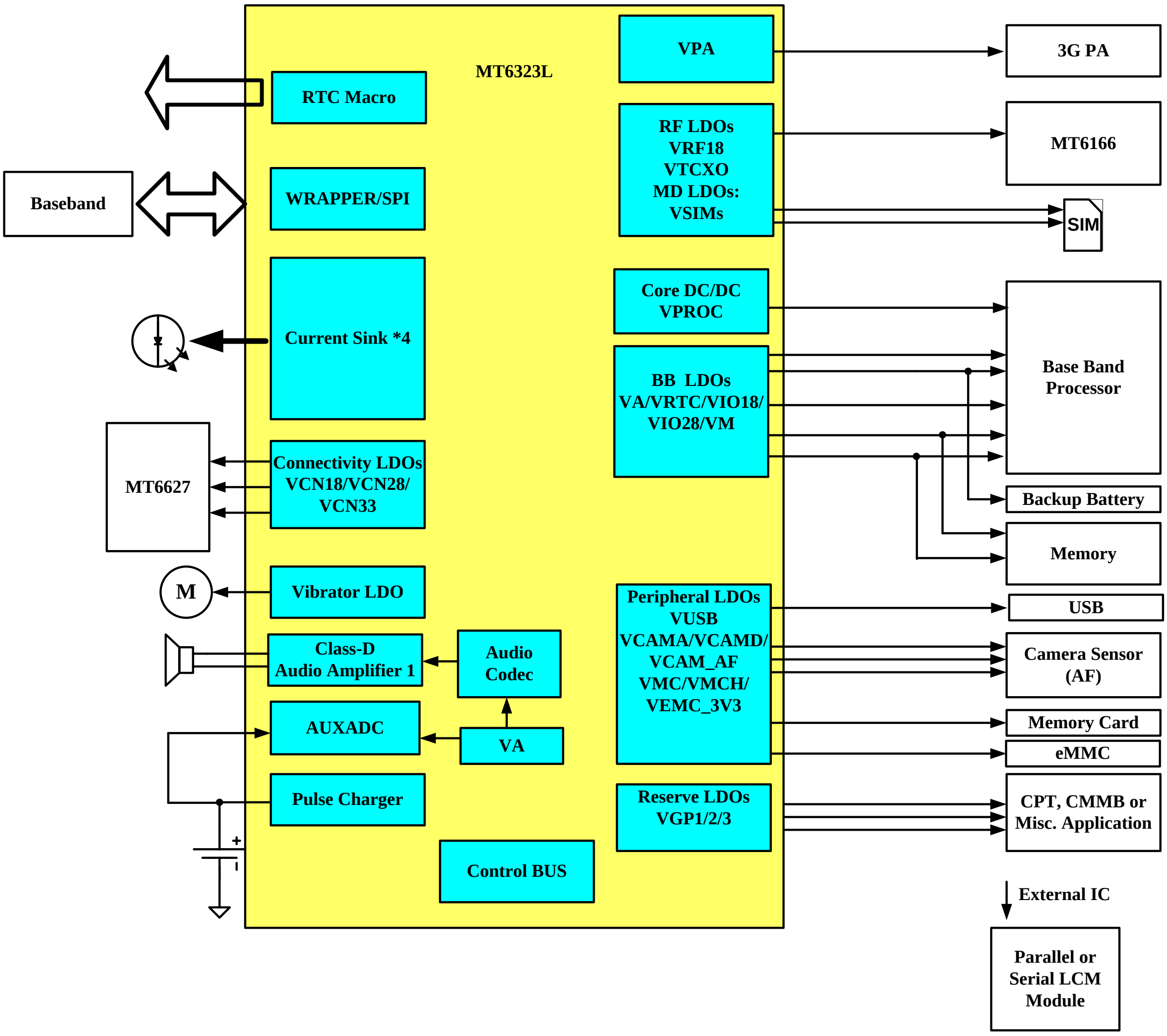

Figure 3-1. MT6323L block diagram

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3.2 PMIC Functional Blocks

MT6323L manages the power supply of the whole chip, such as the baseband, processor, memory, SIM cards, camera, vibrator, etc. MT6323L includes the following analog functions for the use on tablet platforms.

- LDO and BUCK: Provide regulated lower output voltage level from Li-Ion battery
- Current sink (ISINK) driver: Sink current for indicator LED and LCM module
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- Charger controller: Controls/Protects battery charging procedure
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC and high-power/quality audio amplifier
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ 3.3V) nor in the thermal condition, there are 3 methods to power on the handset system.

1) Pulling PWRKEY low (User presses PWRKEY)
2) Setting BBWAKEUP high
3) Valid charger plug-in

Power on/off sequence

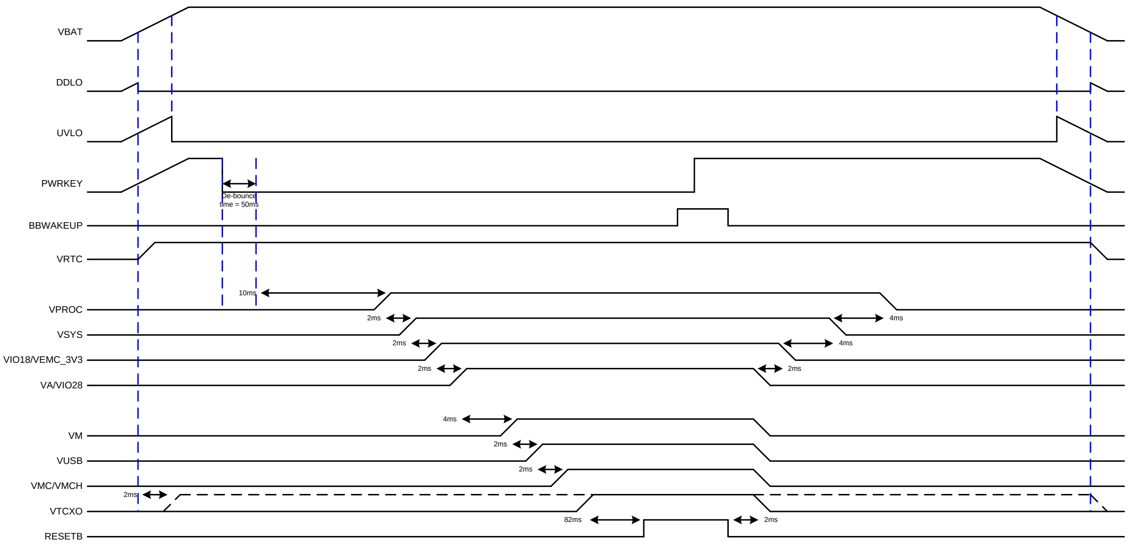

Figure 3-2. Power-on/off control sequence wi/wo XTAL and without EXT_PMIC by pressing PWRKEY

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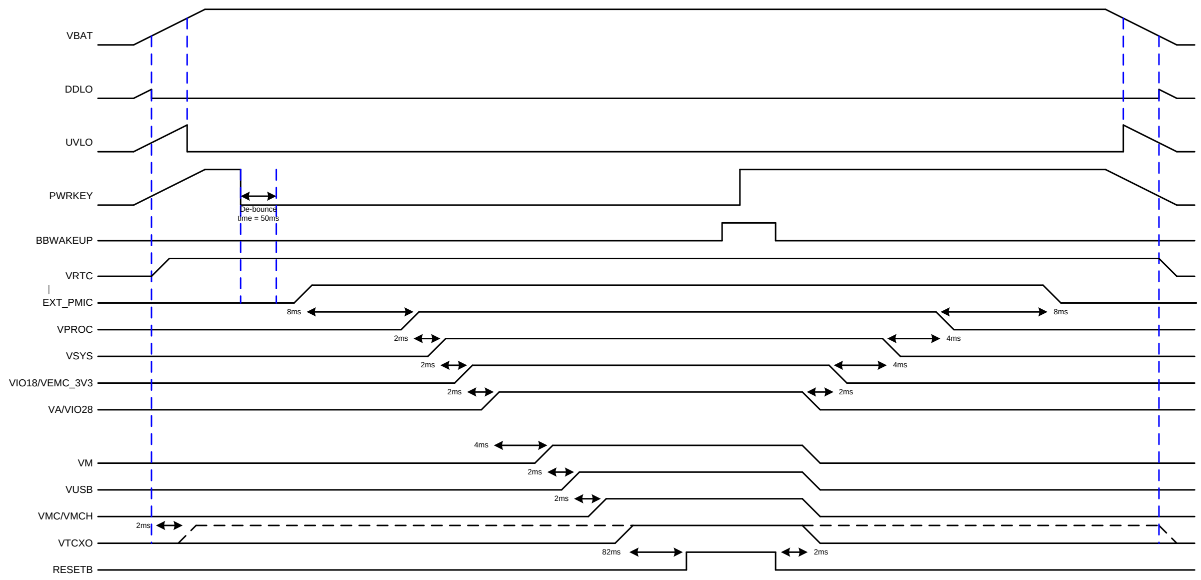

Figure 3-3. Power-on/off control sequence wi/wo XTAL and with EXT_PMIC by pressing PWRKEY

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the BBWAKEUP signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives BBWAKEUP from the baseband.

2. RTC module generates BBWAKEUP to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the BBWAKEUP signal will be directly sent to PMIC. In this case, BBWAKEUP becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. However, if the battery voltage is too low (UVLO state) to power on the handset, the system will not be turned on by any of the three methods. In this case, the charger will charge the battery first, and the handset will be powered on automatically as long as the battery voltage is high enough.

Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below the 3.2V threshold. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

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Within XTAL removal feature, VTCXO LDO is always turned on when VBAT is above the DDLO threshold.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below 2.5V. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Battery Charger (Charger Controller)

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector resists higher input voltages than other parts of PMIC.

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3.2.2.1 Block Descriptions

Charger block diagram

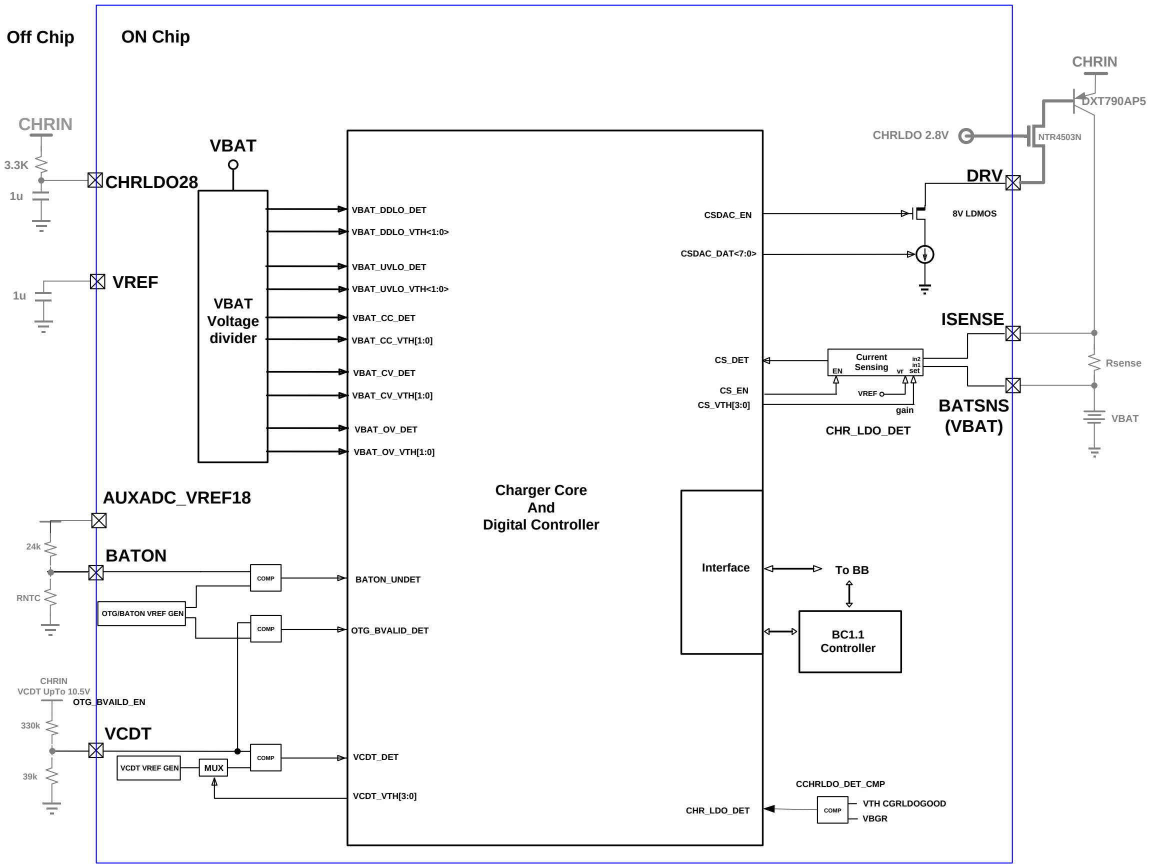

Figure 3-3. PCHR block diagram

3.2.2.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0V), the charger detector will stop the charging process immediately to avoid burning out the chip or even the tablet. Furthermore, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

3.2.2.1.2 Charging Control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.2V, PMIC power-off state), CC mode (constant current mode or fast charging mode at the range of 3.2V < VBAT < 4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging states diagram.

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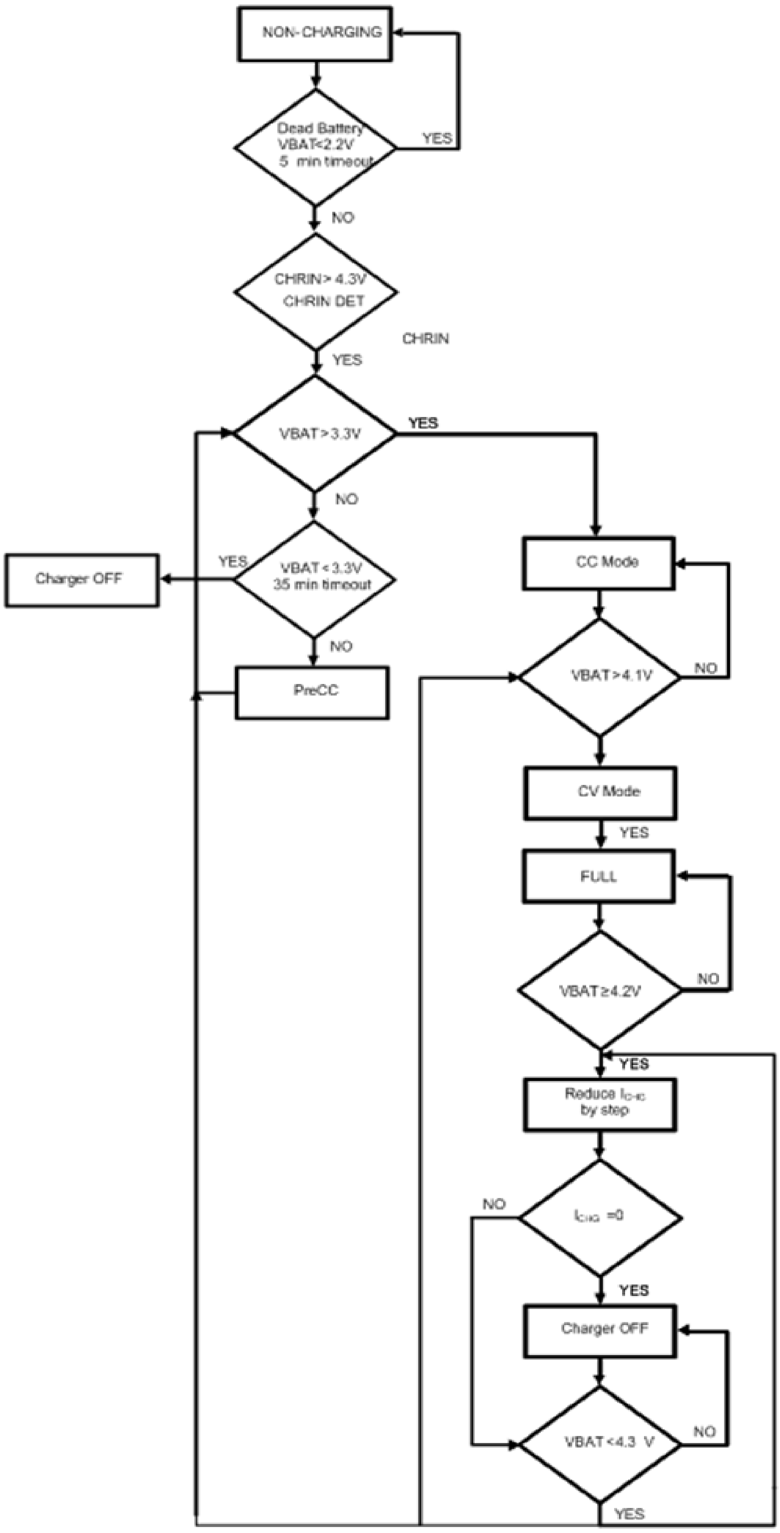

Figure 3-4. Charging states diagram

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Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, IUNIT trickle charging current is applied to the battery.

The IUNIT trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 60mV (AC charger) or 14mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC1,\,AC\ adapter} = \frac{V_{SENSE}}{Rsense} = \frac{60mV}{Rsense}$$

$$I_{PRECC1,\,USBHOST} = \frac{V_{SENSE}}{Rsense} = \frac{14mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.3V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.2ohm, the CC mode charging current can be set from 70 to 1,600mA. It can accommodate the battery charger to various charger inputs with different current capability.

Constant-voltage mode and over-voltage protection (OV)

While the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. While the battery voltage actually reaches 4.2V, the charging current is gradually decreased step-by-step, the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches zero automatically and this mechanism is optimized for different battery packs. Whenever the battery voltage exceeds 4.3V (programmed by SW), a hardware OV protection is activated and turns off the charger immediately.

3.2.2.1.3 BC1.1 Dead-Battery Support

MT6323L also supports dead-battery condition BC1.1. These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after applying the trickle current, the charger will be disabled. On the other hand, once the battery voltage rises up to above 2.2V, the charger will enter the

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PRECC1 stage, and the charging current will be 70mA or 300mA depending on the type of the charging port.

When the battery is below 3.3V, the charger will charge the battery with the PRECC1 current.

A dedicated 5 mins. (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35 mins. (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.3V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

3.2.2.1.4 Auto Power-On Mode (USB DL without battery)

MT6323L features an default auto power-on mode (or USB DL without battery) no matter with or without battery. Users can disable auto power-on by adding external pull-high resistor on the DL_KEY pin. They can still initiate USB DL (auto power-on) by pressing DL_KEY or under valid BAT_ON information (decided by customers' PCB options). Nonetheless, the DL_KEY can support key function in normal mode. The valid BAT_ON information can be detected through battery's NTC when it is connected to the pin BAT_ON of MT6323L.

3.2.3 Buck Converter

There are 3 buck converters in MT6323L to efficiently generate regulated power for processor, digital core, 3G power amplifier and system LDO. The block diagram is shown in Figure 3-1. The buck converters operate with typically 2MHz (V3GPA) and 3MHz (VPROC, VSYS) fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters pulse frequency modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal over-current protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

Table 3-1. Buck converter brief specifications

BUCK name	Vout (Volt)	Imax (mA)	Application
VPROC	0.7~1.3V/1.35V(optional) (6.25mV/step)	2,800	Processor/Digital Core
VSYS	2.2	1,400	System LDO input
VPA	0.5V ~ 3.4V (0.1V/step)	600	3G power amplifier

1. Processor, Digital CORE power VPROC

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VPROC is a high-current buck converter to provide a highly-efficient power supply for the handset processor. Powering from a Li-ion battery, VPROC steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.15V with a maximum load current capability of 2.8A. The output voltage can be adjusted between 0.7V and 1.3V/1.35V(optional). In order to optimize the overall system efficiency for the processor, VPROC features a Dynamic Voltage Frequency Scaling (DVFS) function which allows to dynamically adjust its output voltage under different voltage supply demands from the processor. For more details, refer to the “Dynamic Voltage Frequency Scaling (DVFS)” section.

2. System LDO input power, VSYS
   VSYS is a high-current buck converter to provide a highly-efficient power supply for the system LDO input power. Powering from a Li-ion battery, VSYS steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 2.2V with a maximum load current capability of 1.4A.

3. 3G PA power, VPA
   VPA regulator is a DC-DC step-down converter which provides 0.5V to 3.4V programmable output voltage (0.1V per step) and sources 600mA current at 3.4V and 100mA at 0.5V for 3G PA application.

3.2.4 Low Dropout Regulator (LDOs) and Reference

MT6323L integrates 24 LDOs optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

A low-dropout regulator (LDO) is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to a very small difference between input and output voltages.

There are several features in the design of LDO, including discharge control, soft start and current limit. Before LDO is enabled, the output pin of LDO should be discharged first to avoid voltage accumulation on the capacitance. Soft-start limits inrush current and controls output-voltage rise time during power-up. Current limit is the current protection to limit LDO’s output current and power dissipation.

There are three types of LDOs in the MT6323L PMIC. The analog LDO is optimized for low-frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier. The digital IO LDO is a linear regulator optimized for very low quiescent current. The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features the reverse current protection and is optimized for ultra-low quiescent current while sustaining the RTC function as long as possible.

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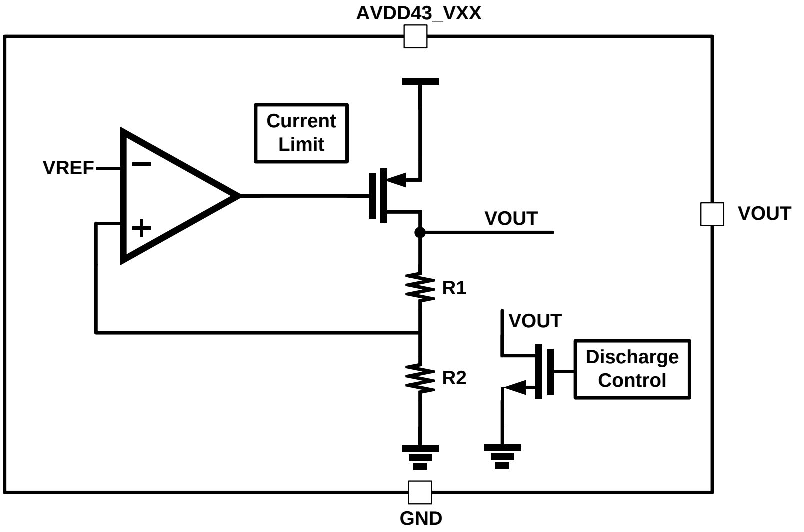

Figure 3-5. LDO block diagram

Table 3-2. LDO types and brief specifications

Type	LDO name	Vout (Volt)	Imax (mA)	Application
ALDO	VCN28	2.8	30	RF chip
ALDO	VTCXO	2.8	40	13/26MHz reference clock
ALDO	VA	2.8	150	Analog baseband
ALDO	VCAMA	2.8	150	Analog power for camera module
DLDO	VCN_3V3	3.3/3.4/3.5/3.6	240	WIFI
DLDO	VIO28	2.8	200	Digital IO
DLDO	VSIM1	1.8/3.0	50	1st SIM card
DLDO	VSIM2	1.8/3.0	50	2nd SIM card
DLDO	VUSB	3.3	20	USB
DLDO	VGP1	1.2/1.3/1.5/1.8/2.0 2.8/3.0/3.3	100	General purpose LDO
DLDO	VGP2	1.2/1.3/1.5/1.8/2.0 /2.5/2.8/3.0	100	General purpose LDO
DLDO	VEMC_3V3	3.0/3.3	400	3.3V EMMC
DLDO	VCAM_AF	1.2/1.3/1.5/1.8/2.0 2.8/3.0/3.3	100	AF application
DLDO	VMC	1.8/3.3	100	SD 2.0/3.0 memory card
DLDO	VMCH	3.0/3.3	400	SD 3.0 memory card
DLDO	VIBR	1.2/1.3/1.5/1.8/2.0 2.8/3.0/3.3	100	Vibrator

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Type	LDO name	Vout (Volt)	Imax (mA)	Application
RTCLDO	VRTC	2.8	2	Real-time clock
VSYS LDO	VM	1.24/1.39/1.54/1.84	700	Memory power
VSYS LDO	VRF18	1.825	200	RF application
VSYS LDO	VIO18	1.8	300	IO pad power
VSYS LDO	VCAMD	1.2/1.3/1.5/1.8	150	Camera application
VSYS LDO	VCAM_IO	1.8	100	Camera IO application
VSYS LDO	VGP3	1.2/1.3/1.5/1.8	200	General purpose LDO
VSYS LDO	VCN18	1.8	120	General purpose LDO

1. Digital IO LDO (VIO28)
   The digital IO LDO is a regulator that sources 200mA (max.) with fixed 2.8V output voltage. The LDO supplies the BB circuitry in the handset and is optimized for a very low quiescent current. The VIO28 LDO is powered on as soon as the system enters the switched-on/stand-by mode. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

2. eMMC LDO (VEMC_3V3)
   VEMC_3V3 and VEMC_1V8 LDOs are regulators used to supply eMMC memory module that will power on as soon as the system enters the switched-on/stand-by mode. They are optimized for a very low quiescent current. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

3. LDO (VGP1/VGP2)
   The general-purpose LDOs are regulators that are designed to source 100mA (max.) with programmable output voltage. The LDOs are reserved to supply the external modules in the handset and is optimized for a very low quiescent current. General-purpose LDOs can be enabled through the SPI interface.

4. Vibrator power LDO (VIBR)
   The vibrator power LDO is a regulator that sources 100mA (max.) with programmable output voltage. The LDO supplies the vibrator circuitry in the handset and is optimized for a low-quiescent current. VIBR LDO can be enabled through the SPI interface. Besides, the folded-back OC protection is also available.

5. AF application LDO (VCAM_AF)
   The AF application LDO is a regulator that sources 100mA (max.) with programmable output voltage.

6. Memory card power LDO (VMC)
   The memory card power LDO is a regulator that sources 100mA (max.) with programmable output voltage. The LDO supplies the memory card circuitry in the handset and is optimized for a low-

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quiescent current. VMC LDO will power on as soon as the system enters the switched-on/stand-by mode. Besides, the folded-back OC protection is also available.

7. SD3.0 memory card power LDO (VMCH)
   The SD3.0 memory card power LDO is a regulator that sources 400mA (max.) with programmable output voltage. The LDO supplies the SD3.0 memory card circuitry in the handset and is optimized for a low-quiescent current. VMCH LDO will power on as soon as the system enters the switched-on/stand-by. Besides, the folded-back OC protection is also available.

8. SIM LDO (VSIM1)
   The SIM LDO is a regulator that sources 50 mA (max.) based on the supply specs of subscriber identity module (SIM) card. The VSIM1 LDO supplies the SIMs in the handset and is controlled independently of the other LDOs. Besides, the folded-back OC protection is also available.

9. 2nd SIM LDO (VSIM2)
   The SIM LDO is a regulator that sources 50mA (max.) with programmable output voltages based on the supply specs of subscriber identity module (SIM) card. The VSIM2 LDO supplies the second SIM card in the handset and is controlled independently of the other LDOs. Besides, the folded-back OC protection is also available.

10. Analog camera LDO (VCAMA)
    The analog camera LDO is a regulator that sources 150mA (max.) with programmable 1.5/1.8/2.5/2.8V output voltage. The LDO supplies the camera circuitry in the handset and is optimized for a very low frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier at 217Hz. VCAMA LDO can be enabled through the SPI interface. Besides, the folded-back OC protection is also available.

11. Analog LDO (VA)
    The analog LDO is a regulator that sources 150mA (max.) output voltage. The LDO supplies the analog sections of the BB chipsets and is optimized for low-frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier at 217Hz. VA LDO is powered on as soon as the system enters the switched-on/stand-by mode. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

12. TCXO LDO (VTCXO)
    TCXO LDO is a regulator that sources 40mA (max.) with a 2.8V output voltage. The LDO supplies the temperature compensated crystal oscillator, which needs its own ultra-low noise supply and very good ripple rejection ratio.

13. GPS LDO (VCN28)
    The analog LDO is a regulator that sources 30mA (max.) with fixed 2.8V output voltage. The LDO supplies the GPS in the handset

14. WIFI LDO (VCN_3V3)

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The analog LDO is a regulator that sources 240mA (max.) with 3.3/3.4/3.5/3.6V output voltage. The LDO supplies the WIFI in the handset

15. USB LDO (VUSB)
    The digital IO LDO is a regulator that sources 20mA (max.) with fixed 3.3V output voltage. The LDO supplies the BB circuitry in the handset and is optimized for a very low quiescent current. VIO LDO is powered on as soon as the system enters the switched-on/stand-by mode. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

16. RTC LDO (VRTC)
    PMIC features a RTC LDO that keeps RTC alive for a long time after the battery has been removed. The LDO charges a backup battery on the BAT_BACKUP pin to ~ 2.8V. In addition, when the battery is removed, it prevents the backup battery from leaking back to VBAT. When the backup battery is fully charged, the high backup battery voltage, low reverse current leakage.

17. Reference voltage output (VREF)
    The reference voltage output is a low-noise, high-PSRR and high-precision reference with a guaranteed accuracy of 1.5% over temperature. The output is used as the system's reference for MT6323L internally. For accurate regulator and charger output voltage, DO NOT load the reference voltage. Bypass it to GND with a minimum 100nF external capacitor.

18. Memory Power (VM)
    VM is a high-current buck converter to provide a highly-efficient power supply for the handset's external memory power (DDR2 and DDR3). Powering from a Li-ion battery, VM steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.24V/1.35V/1.5V/1.84V.

19. IO Power (VIO18)
    VIO18 is a high-current buck converter to provide a highly-efficient power supply for the handset's I/O power. Powering from a Li-ion battery, VIO18 steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.8V with a maximum load current capability of 300mA.

20. RF Power (VRF18)
    VRF18 is a buck converter to provide a highly-efficient power supply for the handset's RF power. Powering from a Li-ion battery, VRF18 steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.825V with a maximum load current capability of 200mA.

21. LDO (VGP3)
    VGP3 is a buck converter to provide a highly-efficient power supply for the handset's module power. Powering from a Li-ion battery, VGP3 steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.2/1.3/1.5/1.8V with a maximum load current capability of 200mA.

22. Digital camera LDO (VCAMD)

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VCAMD is a buck converter to provide a highly-efficient power supply for the handset's camera power. Powering from a Li-ion battery, VCAMD steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.2/1.3/1.5/1.8V with a maximum load current capability of 150mA.

23. LDO (VCAM_IO)
    VCAM_IO is a buck converter to provide a highly-efficient power supply for the handset's camera IO power. Powering from a Li-ion battery, VCAM_IO steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.8V with a maximum load current capability of 100mA.

24. LDO (VCN18)
    VCN18 is a buck converter to provide a highly-efficient power supply for the handset's power. Powering from a Li-ion battery, VCN18 steps down the input voltage from 3.4 ~ 4.4V to the typical output voltage of 1.8V with a maximum load current capability of 120mA.

3.2.5 Drivers

MT6323L supports 4 indicator LED drivers at most. Besides, it provides the drivers for keypad LED and Flash light LED.

3.2.5.1 Indicator LED Driver

For indicator configuration, MT6323L supports up to 4 LEDs with 6-step programmable current in each channel. The LEDs are supplied by the battery voltage. The LED current are controlled by the current sinks in MT6323L. The brightness of the LEDs can be controlled by tuning the current for current sinks or switching on/off the current sinks through dimming control. The dimming frequency and duty can be programmed by registers through the SPI interface. For more details, refer to the "Dimming Control" section.

3.2.5.2 Dimming Control

The intensity of the backlight WLED and keypad LED, which can be adjusted by dimming control. Although they can be controlled separately, the concepts are the same. It can be controlled by programming some internal registers to change the on/off pulse duty cycle and frequency.

3.2.5.2.1 Pulse Duty Cycle

For all drivers, the output duty cycle is adjusted by selecting the corresponding driver's PWM_DUTY value according to the following relationship:

(VIBR/KP/FLASH/BL) PWM duty cycle = (PWM_DUTY + 1) high's , and 32 - (PWM_DUTY +1) low's

, where PWM_DUTY ranges from 0 to 31.

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3.2.5.2.2 Frequency

For all drivers, the output frequency is changed by adjusting the corresponding driver's PWM_DIV value according to the following relationship:

(ISINK) PWM frequency = 1M/(PWM_DIV + 1)/32

, where PWM_DIV is 0~312499.

For FLASH, the output frequency is changed by adjusting PWM_DIV. The output frequency is governed by:

(FLASH/KP) PWM frequency = 1M/(PWM_DIV + 1)/32

, where PWM_DIV ranges from 0 to 255.

3.2.6 Audio CODEC and Accessory Detection

3.2.6.1 Block Descriptions

The block diagram of audio codec is illustrated below. The audio uplink path is composed of PGA and audio ADC. There are three input pairs of the uplink path to support dual-MIC, earphone-MIC and digital MIC. The audio downlink is composed of stereo audio DACs, stereo headphone drivers and mono voice drivers. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.

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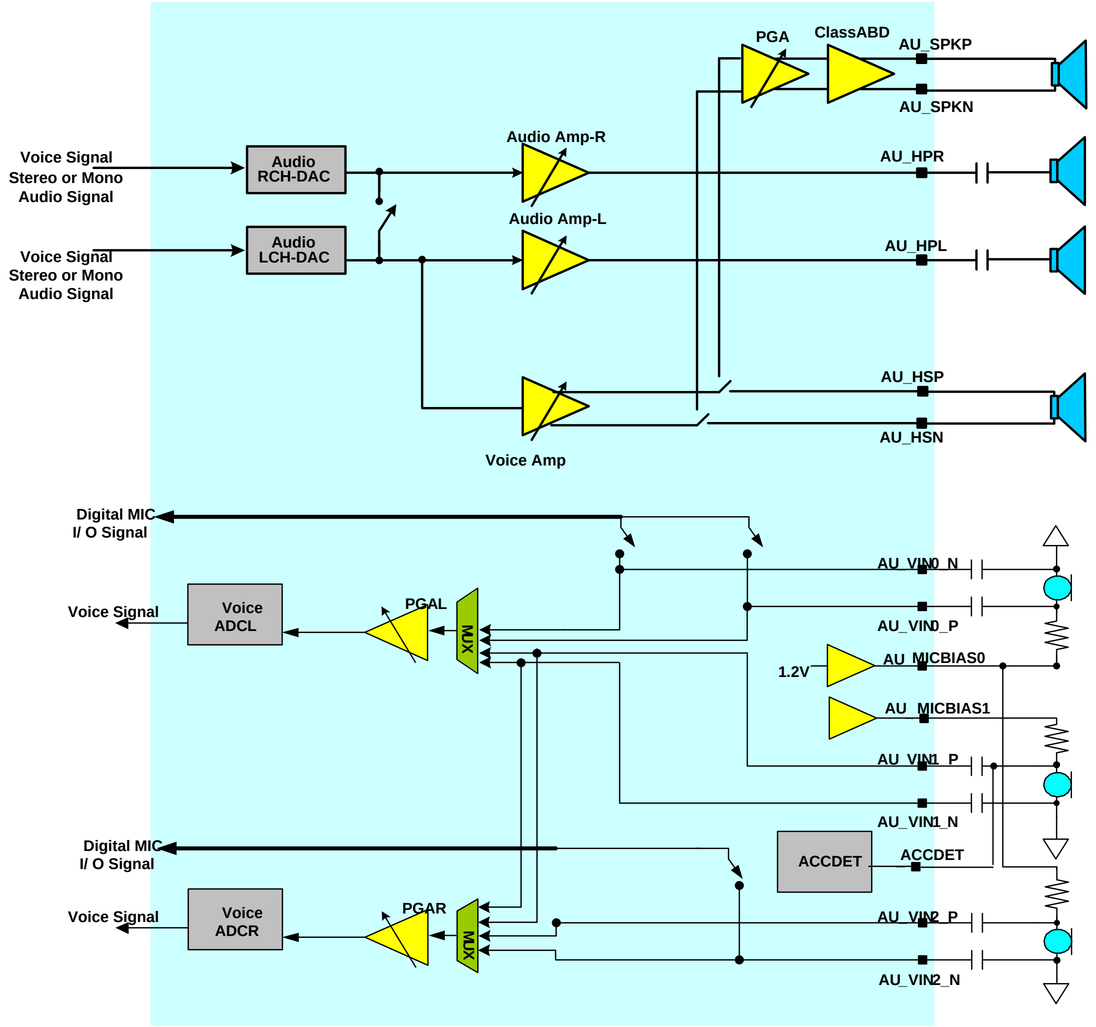

3.2.6.2 Functional Specifications

Symbol	Parameter	Min.	Typical	Max.	Unit
T	Operating temperature	-20		80	°C
VMIC	Microphone biasing voltage		1.9		V
IMIC	Current draw from microphone bias		2		mA
Uplink path					
Analog MIC path					
IDC	Current consumption for single channel		1.5		mA
SNDR	Signal to noise and distortion ratio Input Level: -60 dbm0 Input Level: 0 dbm0	 19 74			 dB dB
RIN	Input impedance (differential)	13	20	27	KΩ
ICN	Idle channel noise			-67	dBm0
xTalk	Crosstalk level			-66	dBm0

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Symbol	Parameter	Min.	Typical	Max.	Unit
Digital MIC path					
DCLK	DMIC clock frequency		1.625/ 3.25		MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 80p)		10		ns
DCFT	DMIC clock fall time (MaxCL = 80p)		10		ns
ICDD	Input capacitance for DMIC data			45	pF

Voice downlink specifications

Symbol	Parameter	Min.	Typical	Max.	Unit
SINAD	Signal to noise and distortion ratio Input Level: -40 dBm0 Input Level: 0 dBm0	 29 	 69		 dB dB
RLOAD	Output resistor load (differential)	16	32		Ω
CLOAD	Output capacitor load			500	pF
ICN	Idle channel noise of transmit path			-67	dBm0
XT	Crosstalk level on transmit path			-66	dBm0

Audio downlink specifications

Symbol	Parameter	Min.	Typical	Max.	Unit
FCK	Clock frequency		6.5		MHz
Fs	Sampling rate	32	44.1	48	kHz
AVDD	Power supply	2.6	2.8	3.1	V
T	Operating temperature	-20		80	°C
IDC	Current consumption		5		mA
PSNR	Peak signal to noise ratio		80		dB
DR	Dynamic range		80		dB
VOUT	Output swing for 0dBFS input level		0.85		Vrms
THD	Total harmonic distortion 11mW at 64 Ω load			-60	dB
RLOAD	Output resistor load (single-ended)		64		Ω
CLOAD	Output capacitor load			250	pF
XT	L-R channel crosstalk		70		dB

3.2.7 Class-AB/D Audio Amplifier

MT6323L has built-in one channel high efficiency class AB/D audio power amplifier capable of delivering 0.7 watt of power on an 8 ohm BTL load from a 3.7V battery supply. Over-current protection is integrated. MT6323L also has built-in receiver mode for 2-in-1 loudspeaker. This built–in receiver

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mode supports multi-purpose loudspeaker without any extra BOM cost. The output power can reach 97mW onto 8 ohm speaker load. The block diagram is shown below.

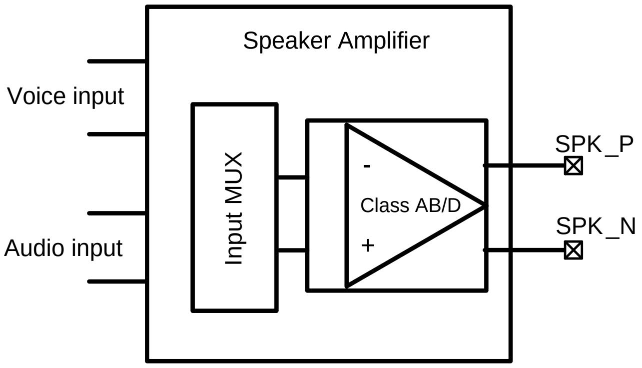

Figure 3-6. Block diagram of class-AB/D

3.2.8 Fuel Gauge

The fuel gauging system includes utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the two measuring methods.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting.

3.2.9 AUXADC

3.2.9.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the sixteen input pins. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data.

Channel	Application	Input range [V]
0	BATSNS	0 ~ 4.5
1	ISENSE	0 ~ 4.5
2	VCDT	0 ~ 1.2
3	BATON	0 ~ 1.8
4	THR_SENSE1	0 ~ 1.2

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Channel	Application	Input range [V]
5	ACCDET	0 ~ 1.8
7	GPS	0 ~ 1.8
others	Internal use	N/A

3.2.9.2 Functional Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Table 3-3. Functional specifications of auxiliary ADC

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		15		Bit
FC	Data rate		1		kHz
CIN	Input capacitance Unselected channel Selected channel			50 1	fF pF
RIN	Input resistance Unselected channel Selected channel	400 1			MΩ MΩ
SNR	Signal to noise ratio		85		dB
T	Operating temperature	-20		80	°C
Iq	Current consumption Power-up Power-down			2 1	mA μA

3.2.10 Real-time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

3.2.10.1 32kHz Crystal Oscillator (XOSC32)

The low-power 32-kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. The key performance is shown in the table below.

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Table 3-4. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power	1.0(*)	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	35	50		%
TR	Rise time on XOSCOUT		TBD		ns/pF
TF	Fall time on XOSCOUT		TBD		ns/pF
	Current consumption			5	μA
T	Operating temperature	-20		80	°C

The minimum VRTC value means if the crystal oscillator starts up successfully, the minimum VRTC for the clock to still be alive is 1V.

Since the crystal parameters determine the oscillation allowance, here are a few recommendations of the crystal parameters to be used well with XOSC32 in MT6323L.

Table 3-5. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min	Typical	Max	Unit
F	Frequency range		32,768		Hz
GL	Drive level			1	uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	KΩ
C0	Static capacitance		0.9	2	pF
CL	Load capacitance	6		12.5	pF

Under such CL range and crystal, the –R is bigger than 3 times. If CL is selected being larger, the frequency accuracy will be decreased, and the –R will degrade too.

3.2.11 Interrupt and Watchdog

3.2.11.1 Interrupt

There are 9 groups of interrupts for MT6323L to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
   - FCHRKEY: Interrupt is issued when FCHRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the FCHR_DEB status to see if it is pressed or released.
2. Thermal interrupt

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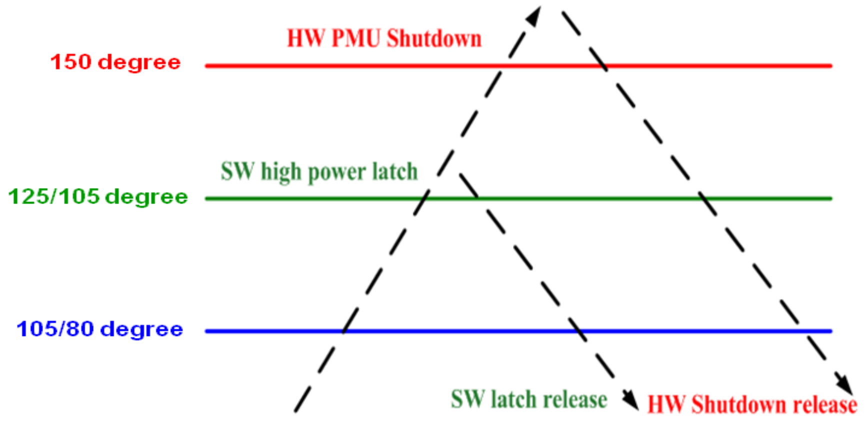
MT6323L issues THR_H interrupt for the software high power latch if PMIC die temperature is over 125°C and issues THR_L for software latch release if PMIC die temperature goes from 125°C back to under 110°C.



3. Charger related interrupt
   There are several interrupts supported for charger control:
   CHRDET
   OV
   WATCHDOG
   BVALID_DET
   VBATON_UNDET

4. Battery voltage/current H/L interrupt
   VBAT detected by AUXADC
   If VBAT is higher than the threshold specified by an register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.

5. Speaker OC interrupt
   MT6323L supports speaker OC interrupt generation which uses PWM detection method.

6. BUCK OC interrupt
   MT6323L has 8 bucks and each has its individual interrupt which uses PWM detection method.
   VPA_OC
   VSYS_OC
   VPROC_OC

7. LDO OC interrupt
   MT6323L supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.

8. RTC interrupt

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9. AUDIO interrupt
   Audio interrupt can inform AP playback of the audio status.

10. ACCDET interrupt
This is for headphone detection.

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Table 3-6. MT6323L interrupt table

STRUP	PWRKEY	RG_INT_EN_PWRKEY	0x0160 bit5	RG_INT_STATUS_PWRKEY	0x0172 bit5	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear
STRUP	FCHRKEY	RG_INT_EN_FCHRKEY	0x0166 bit1	RG_INT_STATUS_FCHRKEY	0x0174 bit1	edge(rising & falling)	0	50ms (in STRUP)	Write 1 Clear
STRUP	THR_H	RG_INT_EN_THR_H	0x0160 bit7	RG_INT_STATUS_THR_H	0x0172 bit7	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
STRUP	THR_L	RG_INT_EN_THR_L	0x0160 bit6	RG_INT_STATUS_THR_L	0x0172 bit6	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
Charger	CHRDET	RG_INT_EN_CHRDET	0x0160 bit10	RG_INT_STATUS_CHRDET	0x0172 bit10	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear
Charger	OV	RG_INT_EN_OV	0x0160 bit11	RG_INT_STATUS_OV	0x0172 bit11	edge(rising)	1	4us (in PCHR_DIG)	Write 1 Clear
Charger	BVALID_DET	RG_INT_EN_BVALID_DET	0x0160 bit9	RG_INT_STATUS_BVALID_DET	0x0172 bit9	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	VBATON_UNDET	RG_INT_EN_VBATON_UNDET	0x0160 bit8	RG_INT_STATUS_VBATON_UNDET	0x0172 bit8	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	WATCHDOG	RG_INT_EN_WATCHDOG	0x0160 bit4	RG_INT_STATUS_WATCHDOG	0x0172 bit4	level (high active)	1	No	Write 1 Clear
Auxadc	BAT_H	RG_INT_EN_BAT_H	0x0160 bit3	RG_INT_STATUS_BAT_H	0x0172 bit3	level (high active)	0	V (in AUXADC)	Write 1 Clear
Auxadc	BAT_L	RG_INT_EN_BAT_L	0x0160 bit2	RG_INT_STATUS_BAT_L	0x0172 bit2	level (high active)	0	V (in AUXADC)	Write 1 Clear
Speaker	SPKL	RG_INT_EN_SPKL	0x0160 bit1	RG_INT_STATUS_SPKL	0x0172 bit1	level (high active)	0	V (in SPK)	Write 1 Clear
Speaker	SPKL_AB	RG_INT_EN_SPKL_AB	0x0160 bit0	RG_INT_STATUS_SPKL_AB	0x0172 bit0	level (high active)	0	V (in SPK)	Write 1 Clear
RTC	RTC	RG_INT_EN_RTC	0x0166 bit4	RG_INT_STATUS_RTC	0x0174 bit4	level (low active)	0	No	Write 1 Clear
Audio	AUDIO	RG_INT_EN_AUDIO	0x0166 bit3	RG_INT_STATUS_AUDIO	0x0174 bit3	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET	RG_INT_EN_ACCDET	0x0166 bit2	RG_INT_STATUS_ACCDET	0x0174 bit2	level (high active)	0	No	Write 1 Clear
Regulator	VPA_OC	RG_INT_EN_VPA	0x0166 bit7	RG_INT_STATUS_VPA	0x0174 bit7	level (high active)	0	PMW deb (in INTCTRL)	Write 1 Clear
Regulator	VSYS_OC	RG_INT_EN_VSYS	0x0166 bit6	RG_INT_STATUS_VSYS	0x0174 bit6	level (high active)	0	PMW deb (in INTCTRL)	Write 1 Clear
Regulator	VPROC_OC	RG_INT_EN_VPROC	0x0166 bit5	RG_INT_STATUS_VPROC	0x0174 bit5	level (high active)	0	PMW deb (in INTCTRL)	Write 1 Clear
LDO	LDO_OC	RG_INT_EN_LDO	0x0166 bit0	RG_INT_STATUS_LDO	0x0174 bit0	level (high active)	1	100/200/400/800us (in INTCTRL)	Write 1 Clear

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3.2.11.2 Watchdog

Watchdog is used to monitor whether the baseband is still awake while charging. The user can set up the time-out threshold by TIMEOUT_GEAR. They are 4s, 8s, 16s, and 32s respectively. The figure below is the state diagram of watchdog. Watchdog timer starts to count when the charger enabling register is set. If the software does not write the specific register within designated time, the watchdog will time out and issue interrupts. It means that the watchdog is also one type of interrupt source in addition to those described in 3.2.11.1. The software can select a proper time-out value by setting up the time-out gear register. Like most of the interrupt mechanism mentioned above, the watchdog interrupt is write-clear.

PMIC can start to charge only when the charger is detected, charger enabling register is set, and watchdog is not timed-out. If one of the three conditions is false, the charging will be prohibited.

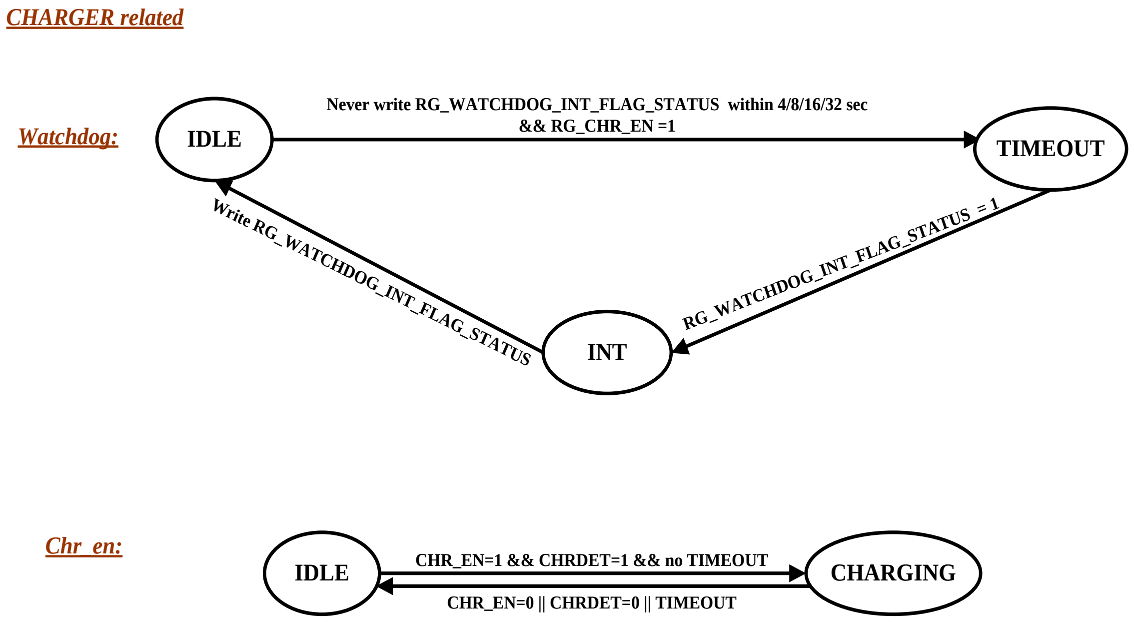

Figure 3-13. Watchdog

3.2.12 SIMLS

The SIM card interface (SIM interface) voltage level shift provides level shifting required for low-voltage GSM controller

There are two SIM card interface modules to support two SIM cards simultaneously in Baseband. SIM card interface go through PMU circuit, then it connects to SIM CARD.The SIMLS circuit meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting for low-voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a

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reset input and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband to the SIM supply (Vsim).

All pins that are connected to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 2kV HBM (Human Body Mode) ESD. In order to ensure proper ESD protection, careful board layout is required.

3.2.12.1 Block Descriptions

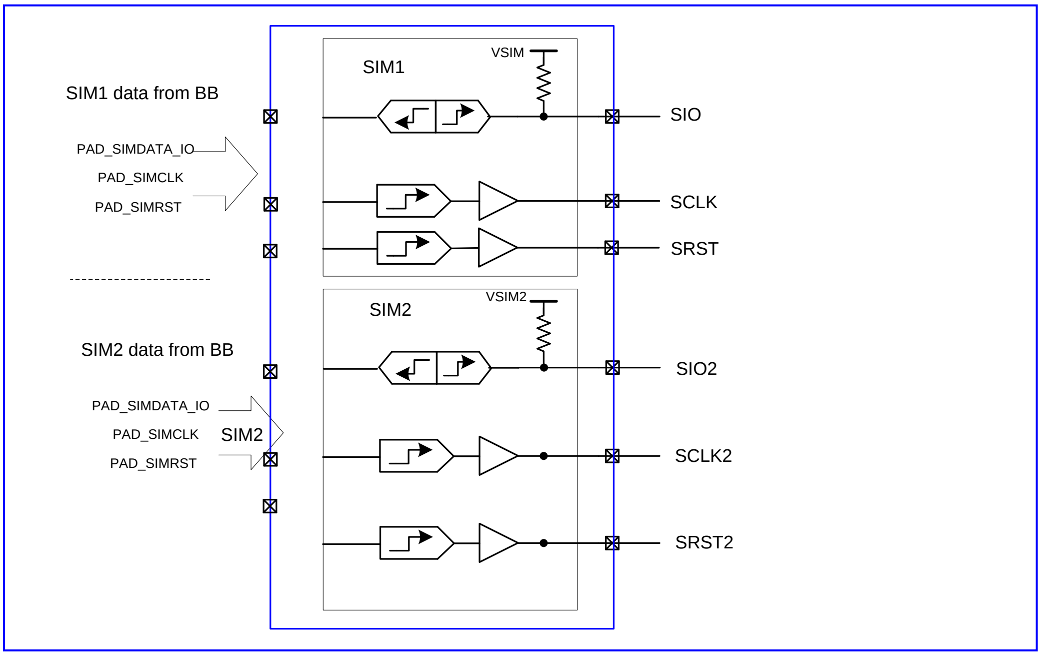

Figure 3-14. SIMLS circuit block diagram

3.2.12.2 Characteristics

Table 3-7. SIMLS specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Interface to 3V SIM card						
	Output low of SRST	I = 200µA			0.36	V
	Output high of SRST	I = -200µA	0.9*VSIM			V
	Output low of SCLK	I = 200µA			0.4	V
	Output high of SCLK	I =-100µA	0.9*VSIM			V
	Input/Output low of SIO	I=-1mA			0.4	V
	Input/Output high of SIO	I = ±20µA	VSIM-0.4			V
	(Iil)Pull high current of SIO	Vil = 0V			-1	mA
Interface to 1.8V SIM card						
	Output low of SRST	I = 200µA			0.2*VSIM	V
	Output high of SRST	I = -200µA	0.9*VSIM			V

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Output low of SCLK	I = 200µA			0.12*VSIM	V
	Output high of SCLK	I = -100µA	0.9*VSIM			V
	Input/Output low of SIO	I=-1mA			0.15*VSIM	V
	Input/Output high of SIO	I=+/-20uA	VSIM-0.4			V
	(Iil)Pull high current of SIO	ViL=0V			-1	mA
SIM card interface timing						
	SIO pull-up resistance to VSIM		4	5	6	kΩ
	SRST, SIO rise/fall times	VSIM = 3, 1.8V, load with 30pF			1	µs
	SCLK rise/fall times	VSIM = 3V, CLK load with 30pF			18	ns
		VSIM = 1.8V, CLK load with 30pF			50	ns
	SCLK frequency	CLK load with 30pF			5	MHz
	SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5MHz	47		53	%

Ablility of driving of SIM1_SIO and SIM2_SIO are from the PAD of SIMx_SIO on BB.

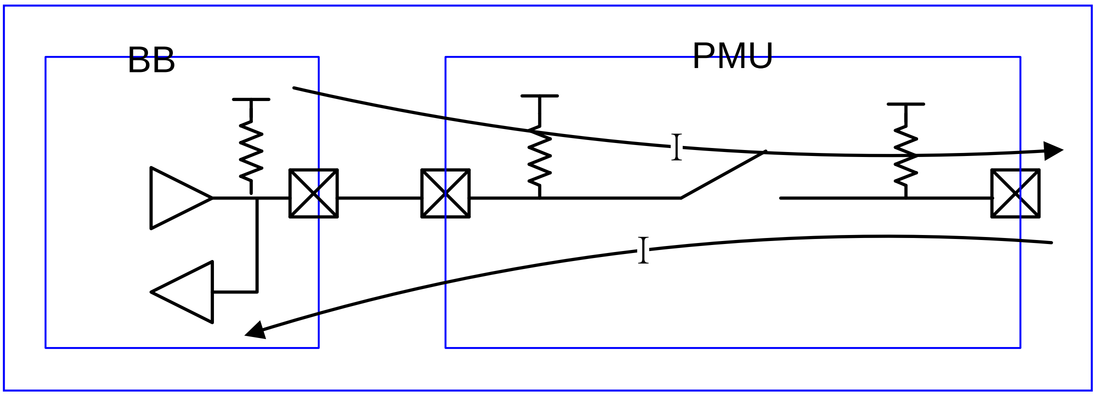

Figure 3-15. SIMIO circuit

3.2.13 SPI Interface

PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

3.2.13.1 Data Format

The pre-defined SPI format consists of two mode: Single I/O mode and dual I/O mode. Single I/O always use MOSI and MISO as output and input respectively. Dual I/O use both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction,

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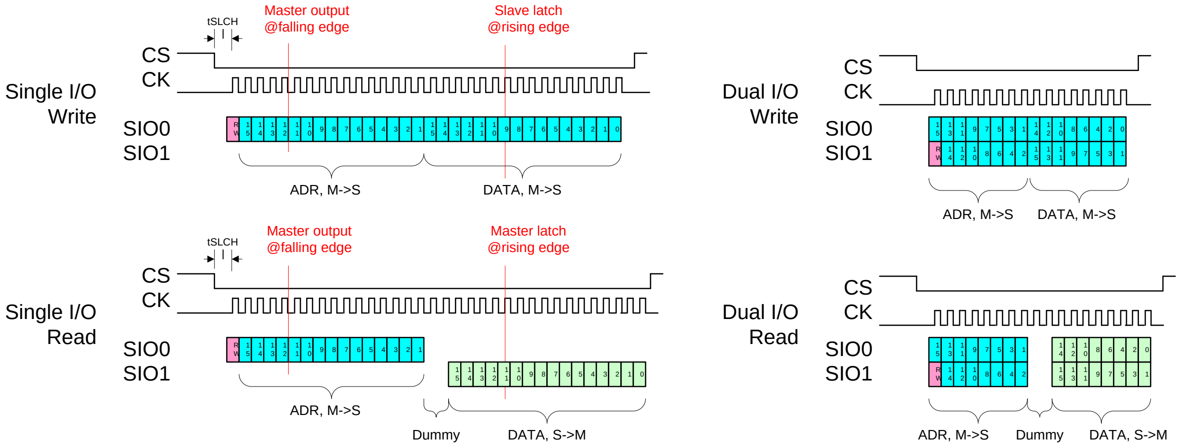
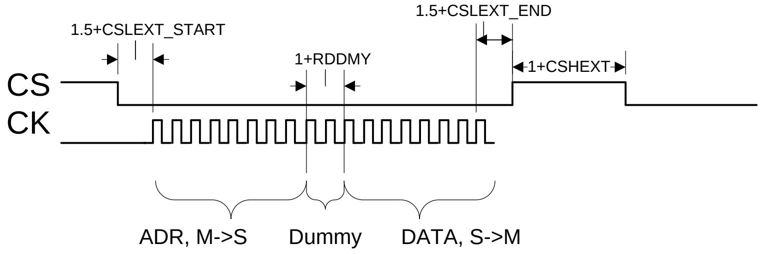
15-bit address (bit 14 to bit 0) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master at rising edge of clock, and output data at falling edge of clock. The parameter tCSLEXT_START, tRDMMY and tCSLEXT_END are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

SPI format:



SPI parameter configuration:



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3.2.14 GPIO List

Table 3-8. MT6323L GPIO list

Pin Name	Aux Func.0	Aux Func.1	PU/PD	PullEn	PullSel	Mode
PAD_INT	GPIO0	**O:INT**	PU/**PD**	1	0	1
PAD_SRCLKEN	GPIO1	**I1:SRCLKEN**	PU/**PD**	1	0	1
PAD_RTC_32K1V8	GPIO2	**O:RTC_32K1V8**	PU/PD	0		1
PAD_SPI_CLK	GPIO3	**I0:SPI_CLK**	PU/**PD**	1	0	1
PAD_SPI_CSN	GPIO4	**I1:SPI_CSN**	**PU**/PD	1	1	1
PAD_SPI_MOSI	GPIO5	**B0:SPI_MOSI**	PU/**PD**	1	0	1
PAD_SPI_MISO	GPIO6	**B0:SPI_MISO**	PU/**PD**	1	0	1
PAD_AUD_CLK	GPIO7	**I0:AUD_CLK**	PU/**PD**	1	0	1
PAD_AUD_MOSI	GPIO8	**I0:AUD_MOSI**	PU/**PD**	1	0	1
PAD_AUD_MISO	GPIO9	**O:AUD_MISO**	PU/**PD**	1	0	1
PAD_SIM1_AP_SCLK	GPIO10	**I0:SIM1_AP_SCLK**	PU/PD	0		1
PAD_SIM1_AP_SRST	GPIO11	**I0:SIM1_AP_SRST**	PU/PD	0		1
PAD_SIM2_AP_SCLK	GPIO12	**I0:SIM2_AP_SCLK**	PU/PD	0		1
PAD_SIM2_AP_SRST	GPIO13	**I0:SIM2_AP_SRST**	PU/PD	0		1
PAD_SIMLS1_SCLK	GPIO14	**O:SIMLS1_SCLK**	PU/PD	0		1
PAD_SIMLS1_SRST	GPIO15	**O:SIMLS1_SRST**	PU/PD	0		1
PAD_SIMLS2_SCLK	GPIO16	**O:SIMLS2_SCLK**	PU/PD	0		1
PAD_SIMLS2_SRST	GPIO17	**O:SIMLS2_SRST**	PU/PD	0		1

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3.2.15 Real Time Clock (RTC)

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768KHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor is used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g., 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

3.2.15.1 RTC Programming Guide

Always turn on AUD_26M before 32k need to be measured.

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3.3 Register Table and Descriptions

Module name: PMIC_REG Base address: (+0h)

Address	Name	Width	Register function
0000	**CHR_CON0**	16	Charger Control Register 0
0002	**CHR_CON1**	16	Charger Control Register 1
0004	**CHR_CON2**	16	Charger Control Register 2
0006	**CHR_CON3**	16	Charger Control Register 3
0008	**CHR_CON4**	16	Charger Control Register 4
000C	**CHR_CON6**	16	Charger Control Register 6
000E	**CHR_CON7**	16	Charger Control Register 7
001A	**CHR_CON13**	16	Charger Control Register 13
001E	**CHR_CON15**	16	Charger Control Register 15
0020	**CHR_CON16**	16	Charger Control Register 16
0022	**CHR_CON17**	16	Charger Control Register 17
0024	**CHR_CON18**	16	Charger Control Register 18
0026	**CHR_CON19**	16	Charger Control Register 19
002C	**CHR_CON22**	16	Charger Control Register 22
002E	**CHR_CON23**	16	Charger Control Register 23
0036	**CHR_CON27**	16	Charger Control Register 27
0038	**CHR_CON28**	16	Charger Control Register 28
003C	**STRUP_CON0**	16	STRUP Control Register 0
003E	**STRUP_CON2**	16	STRUP Control Register 2
0040	**STRUP_CON3**	16	STRUPControl Register 3
0044	**STRUP_CON5**	16	STRUP Control Register 5
004A	**STRUP_CON8**	16	STRUP Control Register 8
004C	**STRUP_CON9**	16	STRUP Control Register 9
004E	**STRUP_CON10**	16	STRUP Control Register 10
0052	**SPK_CON0**	16	Speaker Control Register 0
0056	**SPK_CON2**	16	Speaker Control Register 2
005E	**SPK_CON6**	16	Speaker Control Register 6
0062	**SPK_CON8**	16	Speaker Control Register 8
0064	**SPK_CON9**	16	Speaker Control Register 9
006A	**SPK_CON12**	16	Speaker Control Register 12
011A	**TOP_RST_MISC**	16	Reset Control Misc
0132	**TEST_OUT**	16	TEST_OUT
0142	**CHRSTATUS**	16	CHR Status
0144	**TDSEL_CON**	16	TDSEL_CON
0146	**RDSEL_CON**	16	RDSEL_CON

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Address	Name	Width	Register function
0148	SMT_CON0	16	SMT_CON0
014A	SMT_CON1	16	SMT_CON1
014C	SMT_CON2	16	SMT_CON2
014E	SMT_CON3	16	SMT_CON3
0150	SMT_CON4	16	SMT_CON4
0152	DRV_CON0	16	DRV_CON0
0154	DRV_CON1	16	DRV_CON1
0156	DRV_CON2	16	DRV_CON2
0158	DRV_CON3	16	DRV_CON3
015A	DRV_CON4	16	DRV_CON4
015C	SIMLS1_CON	16	SIMLS1_CON
015E	SIMLS2_CON	16	SIMLS2_CON
0182	FQMTR_CON0	16	Frequency Meter Control Register 0
0184	FQMTR_CON1	16	Frequency Meter Control Register 1
0186	FQMTR_CON2	16	Frequency Meter Control Register 2
0188	RG_SPI_CON	16	SPI Control Register
018A	DEW_DIO_EN	16	Dual I/O Mode Enable
018C	DEW_READ_TEST	16	Read Test
018E	DEW_WRITE_TEST	16	Write Test
0190	DEW_CRC_SWRST	16	CRC_SWRST
0192	DEW_CRC_EN	16	CRC Enable
0194	DEW_CRC_VAL	16	CRC Value
0196	DEW_DBG_MON_SEL	16	Monitor Flag Group Selection
0198	DEW_CIPHER_KEY_SEL	16	CIPHER Key Selection
019A	DEW_CIPHER_IV_SEL	16	CIPHER Initial Vector Selection
019C	DEW_CIPHER_EN	16	CIPHER Engine Enable
019E	DEW_CIPHER_RDY	16	CIPHER Data Ready
01A0	DEW_CIPHER_MODE	16	CIPHER Mode Enable
01A2	DEW_CIPHER_SWRST	16	CIPHER Soft Reset
01A4	DEW_RDDMY_NO	16	Read Dummy Cycle Number
01A6	DEW_RDATA_DLY_SEL	16	Read Data Delay Configuration
021E	VPROC_CON9	16	VPROC Control Register 9
0304	VPA_CON2	16	VPA Control Register 2
030E	VPA_CON7	16	VPA Control Register 7
0312	VPA_CON9	16	VPA Control Register 9
0330	ISINK0_CON0	16	ISINK0 Control Register 0
0332	ISINK0_CON1	16	ISINK0 Control Register 1
0334	ISINK0_CON2	16	ISINK0 Control Register 2
0336	ISINK0_CON3	16	ISINK0 Control Register 3

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Address	Name	Width	Register function
0338	ISINK1_CON0	16	ISINK1 Control Register 0
033A	ISINK1_CON1	16	ISINK1 Control Register 1
033C	ISINK1_CON2	16	ISINK1 Control Register 2
033E	ISINK1_CON3	16	ISINK1 Control Register 3
0340	ISINK2_CON0	16	ISINK2 Control Register 0
0342	ISINK2_CON1	16	ISINK2 Control Register 1
0344	ISINK2_CON2	16	ISINK2 Control Register 2
0346	ISINK2_CON3	16	ISINK2 Control Register 3
0348	ISINK3_CON0	16	ISINK3 Control Register 0
034A	ISINK3_CON1	16	ISINK3 Frequency Register
034C	ISINK3_CON2	16	ISINK3 Control Register 2
034E	ISINK3_CON3	16	ISINK3 Control Register 3
0350	ISINK_ANA0	16	ISINKS ACD Interface 0
0354	ISINK_PHASE_DLY	16	ISINK Phase Delay
0356	ISINK_EN_CTRL	16	ISINK Enable Control
0402	ANALDO_CON1	16	Analog LDO Control Register 1
0404	ANALDO_CON2	16	Analog LDO Control Register 2
0408	ANALDO_CON4	16	Analog LDO Control Register 4
040A	ANALDO_CON5	16	Analog LDO Control Register 5
0410	ANALDO_CON8	16	Analog LDO Control Register 8
0412	ANALDO_CON10	16	Analog LDO Control Register 10
0418	ANALDO_CON17	16	Analog LDO Control Register 17
041C	ANALDO_CON19	16	Analog LDO Control Register 19
041E	ANALDO_CON20	16	Analog LDO Control Register 20
0420	ANALDO_CON21	16	Analog LDO Control Register 21
0500	DIGLDO_CON0	16	Digital LDO control register 0
0502	DIGLDO_CON2	16	Digital LDO control register 2
0504	DIGLDO_CON3	16	Digital LDO control register 3
0506	DIGLDO_CON5	16	Digital LDO control register 5
0508	DIGLDO_CON6	16	Digital LDO control register 6
050A	DIGLDO_CON7	16	Digital LDO control register 7
050C	DIGLDO_CON8	16	Digital LDO control register 8
050E	DIGLDO_CON9	16	Digital LDO control register 9
0512	DIGLDO_CON11	16	Digital LDO Control Register 11
0516	DIGLDO_CON13	16	Digital LDO Control Register 13
0518	DIGLDO_CON14	16	Digital LDO Control Register 14
051A	DIGLDO_CON15	16	Digital LDO Control Register15
0520	DIGLDO_CON18	16	Digital LDO Control Register 18
0522	DIGLDO_CON19	16	Digital LDO Control Register 19

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Address	Name	Width	Register function
0524	DIGLDO_CON20	16	Digital LDO Control Register 20
0530	DIGLDO_CON28	16	Digital LDO Control Register 28
0532	DIGLDO_CON29	16	Digital LDO Control Register 29
0534	DIGLDO_CON30	16	Digital LDO Control Register 30
0536	DIGLDO_CON31	16	Digital LDO Control Register 31
0538	DIGLDO_CON32	16	Digital LDO Control Register 32
053C	DIGLDO_CON34	16	Digital LDO Control Register 34
053E	DIGLDO_CON35	16	Digital LDO Control Register 35
0542	DIGLDO_CON39	16	Digital LDO Control Register 39
0544	DIGLDO_CON40	16	Digital LDO Control Register 40
0548	DIGLDO_CON42	16	Digital LDO Control Register 42
054C	DIGLDO_CON44	16	Digital LDO Control Register 44
054E	DIGLDO_CON45	16	Digital LDO Control Register 45
0552	DIGLDO_CON47	16	Digital LDO Control Register 47
0556	DIGLDO_CON49	16	Digital LDO Control Register 49
055A	DIGLDO_CON51	16	Digital LDO Control Register 51
055C	DIGLDO_CON52	16	Digital LDO Control Register 52
055E	DIGLDO_CON53	16	Digital LDO Control Register 53
0560	DIGLDO_CON54	16	Digital LDO Control Register 54
0600	EFUSE_CON0	16	EFUSE Control Register 0
0602	EFUSE_CON1	16	EFUSE Control Register 1
0604	EFUSE_CON2	16	EFUSE Control Registerr 2
0606	EFUSE_CON3	16	EFUSE Control Register 3
0608	EFUSE_CON4	16	EFUSE Control Register 4
060A	EFUSE_CON5	16	EFUSE Control Register 5
060C	EFUSE_CON6	16	EFUSE Control Register 6
060E	EFUSE_VAL_0_15	16	EFUSE val 0 15
0610	EFUSE_VAL_16_31	16	EFUSE val 16 31
0612	EFUSE_VAL_32_47	16	EFUSE val 32 47
0614	EFUSE_VAL_48_63	16	EFUSE val 48 63
0616	EFUSE_VAL_64_79	16	EFUSE val 64 79
0618	EFUSE_VAL_80_95	16	EFUSE val 80 95
061A	EFUSE_VAL_96_111	16	EFUSE val 96 111
061C	EFUSE_VAL_112_127	16	EFUSE val 112 127
061E	EFUSE_VAL_128_143	16	EFUSE val 128 143
0620	EFUSE_VAL_144_159	16	EFUSE val 144 159
0622	EFUSE_VAL_160_175	16	EFUSE val 160 175
0624	EFUSE_VAL_176_191	16	EFUSE val 176 191
0626	EFUSE_DOUT_0_15	16	EFUSE dout 0 15

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Address	Name	Width	Register function
0628	EFUSE_DOUT_16_31	16	EFUSE dout 16 31
062A	EFUSE_DOUT_32_47	16	EFUSE dout 32 47
062C	EFUSE_DOUT_48_63	16	EFUSE dout 48 63
062E	EFUSE_DOUT_64_79	16	EFUSE dout 64 79
0630	EFUSE_DOUT_80_95	16	EFUSE dout 80 95
0632	EFUSE_DOUT_96_111	16	EFUSE dout 111
0634	EFUSE_DOUT_112_127	16	EFUSE dout 112 127
0636	EFUSE_DOUT_128_143	16	EFUSE dout 128 143
0638	EFUSE_DOUT_144_159	16	EFUSE dout 144 159
063A	EFUSE_DOUT_160_175	16	EFUSE dout 160 175
063C	EFUSE_DOUT_176_191	16	EFUSE dout 176 191
063E	EFUSE_CON7	16	EFUSE Control Register 7
0640	EFUSE_CON8	16	EFUSE Control Register 8
0642	EFUSE_CON9	16	EFUSE Control Register 9
0700	AUDTOP_CON0	16	AUDIO_TOP Config Register 0
0702	AUDTOP_CON1	16	AUDIO_TOP Config Register 1
0704	AUDTOP_CON2	16	AUDIO_TOP Config Register 2
0706	AUDTOP_CON3	16	AUDIO_TOP Config Register 3
0708	AUDTOP_CON4	16	AUDIO_TOP Config Register 4
070A	AUDTOP_CON5	16	AUDIO_TOP Config Register 5
070C	AUDTOP_CON6	16	AUDIO_TOP Config Register 6
070E	AUDTOP_CON7	16	AUDIO_TOP Config Register 7
0710	AUDTOP_CON8	16	AUDIO_TOP Config Register 8
0712	AUDTOP_CON9	16	AUDIO_TOP Config Register 9
0714	AUXADC_ADC0	16	AUXADC ADC Register 0
0716	AUXADC_ADC1	16	AUXADC ADC Register 1
0718	AUXADC_ADC2	16	AUXADC ADC Register 2
071A	AUXADC_ADC3	16	AUXADC ADC Register 3
071C	AUXADC_ADC4	16	AUXADC ADC Register 4
071E	AUXADC_ADC5	16	AUXADC ADC Register 5
0720	AUXADC_ADC6	16	AUXADC ADC Register 6
0722	AUXADC_ADC7	16	AUXADC ADC Register 7
0724	AUXADC_ADC8	16	AUXADC ADC Register 8
0726	AUXADC_ADC9	16	AUXADC ADC Register 9
0728	AUXADC_ADC10	16	AUXADC ADC Register 10
072A	AUXADC_ADC11	16	AUXADC ADC Register 11
072C	AUXADC_ADC12	16	AUXADC ADC Register 12
072E	AUXADC_ADC13	16	AUXADC ADC Register 13
0730	AUXADC_ADC14	16	AUXADC ADC Register 14

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Address	Name	Width	Register function
0732	**AUXADC_ADC15**	16	AUXADC ADC Register 15
0738	**AUXADC_ADC18**	16	AUXADC ADC Register 18
073A	**AUXADC_ADC19**	16	AUXADC ADC Register 19
073C	**AUXADC_ADC20**	16	AUXADC ADC Register 20
074E	**AUXADC_CON6**	16	AUXADC Control Register 6
8000	**RTC_BBPU**	16	Baseband power up
8002	**RTC_IRQ_STA**	16	RTC IRQ status This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
8004	**RTC_IRQ_EN**	16	RTC IRQ enable This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
8006	**RTC_CII_EN**	16	Counter increment IRQ enable This register activates or de-activates the IRQ generation when the TC counter reaches its maximum value.
8008	**RTC_AL_MASK**	16	RTC alarm mask The alarm condition for alarm IRQ generation depends on whether or not the corresponding bit in this register is masked. Warning: If you set all bits 1 in RTC_AL_MASK (i.e. RTC_AL_MASK=0x7f) and PWREN=1 in RTC_BBPU, it means alarm comes EVERY SECOND, not disabled.
800A	**RTC_TC_SEC**	16	RTC seconds time counter register
800C	**RTC_TC_MIN**	16	RTC minutes time counter register
800E	**RTC_TC_HOU**	16	RTC hours time counter register
8010	**RTC_TC_DOM**	16	RTC day-of-month time counter register
8012	**RTC_TC_DOW**	16	RTC day-of-week time counter register
8014	**RTC_TC_MTH**	16	RTC month time counter register
8016	**RTC_TC_YEA**	16	RTC year time counter register
8018	**RTC_AL_SEC**	16	RTC second alarm setting register
801A	**RTC_AL_MIN**	16	RTC minute alarm setting register
801C	**RTC_AL_HOU**	16	RTC hour alarm setting register
801E	**RTC_AL_DOM**	16	RTC day-of-month alarm setting register
8020	**RTC_AL_DOW**	16	RTC day-of-week alarm setting register
8022	**RTC_AL_MTH**	16	RTC month alarm setting register
8024	**RTC_AL_YEA**	16	RTC year alarm setting register
8026	**RTC_OSC32CON**	16	OSC32 control The function is only active when

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Address	Name	Width	Register function
			RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values. When powerkeys do not match, the internal xosccali=0x7.
8028	RTC_POWERKEY1	16	RTC_POWERKEY1 register
802A	RTC_POWERKEY2	16	RTC_POWERKEY2 register
802C	RTC_PDN1	16	PDN1
802E	RTC_PDN2	16	PDN2
8030	RTC_SPAR0	16	Spare register for specific purpose
8032	RTC_SPAR1	16	Spare register for specific purpose
8036	RTC_PROT	16	Lock/unlock scheme to prevent RTC miswriting
8038	RTC_DIFF	16	One-time calibration offset This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
803A	RTC_CALI	16	Repeat calibration offset This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.
803C	RTC_WRTGR	16	Enable the transfers from core to RTC in the queue
803E	RTC_CON	16	Other RTC control register Note: GPU,GOE,LPRST,LPEN are tie0 and GPEN,F32KOB are tie1 internally when RTC_POWERKEY1 & RTC_POWERKEY2 do not match the correct values. After changing the RTC_CON, you have to write WRTGR=1 to take effect.

0000 CHR_CON0 Charger Control Register 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VCDT_HV_DET		RGS_CHRDET	RG_CHR_EN	RG_CSDAC_EN		RGS_CHR_LDO_DET	RG_VCDT_HV_EN
Type									RO		RO	RW	RW		RO	RW
Reset									0		0	0	0		0	1

Bit(s)	Mnemonic	Name	Description
7	RGS_VCDT_HV_DET	RGS_VCDT_HV_DET	**Detects charger-in high voltage (with de-bounce)** 0: Charge-in voltage < VCDT_HV_VTH 1: Charge-in voltage > VCDT_HV_VTH
5	RGS_CHRDET	RGS_CHRDET	**Detects charger-in** 0: No valid charger detected 1: Valid charger detected

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Bit(s)	Mnemonic	Name	Description
4	**RG_CHR_EN**	RG_CHR_EN	**Charger enabling setting, which gates CSDAC_EN, PCHR_AUTO and HWCV_EN** 0: Disable charger 1: Enable charger
3	**RG_CSDAC_EN**	RG_CSDAC_EN	**Enable CS DAC** 0: Disable CS DAC 1: Enable CS DAC
1	**RGS_CHR_LDO_DET**	RGS_CHR_LDO_DET	**Detects charger LDO** If not detected, pulse charger cannot work. 0: Invalid charger LDO 1: Valid charger LDO
0	**RG_VCDT_HV_EN**	RG_VCDT_HV_EN	

0002 CHR_CON1 Charger Control Register 1 00F2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCDT_HV_VTH							
Type									RW							
Reset									1	1	1	1				

Bit(s)	Mnemonic	Name	Description
7:4	**RG_VCDT_HV_VTH**	RG_VCDT_HV_VTH	**ChargerIn HV detection threshold** Default: 4.3/9.5V for VTHL/VTHH 0000~1000: 4.2V~4.6V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step

0004 CHR_CON2 Charger Control Register 2 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VBAT_CC_DET	RGS_VBAT_CV_DET	RGS_CS_DET		RG_CS_EN		RG_VBAT_CV_EN	
Type									RO	RO	RO		RW		RW	
Reset									0	0	0		0		0	

Bit(s)	Mnemonic	Name	Description
7	**RGS_VBAT_CC_DET**	RGS_VBAT_CC_DET	**VBAT voltage detection for CC** 0: VBAT voltage < VBAT_CC_VTH 1: VBAT voltage > VBAT_CC_VTH
6	**RGS_VBAT_CV_DET**	RGS_VBAT_CV_DET	**VBAT voltage detection for CV** 0: VBAT voltage < VBAT_CV_VTH 1: VBAT voltage > VBAT_CV_VTH
5	**RGS_CS_DET**	RGS_CS_DET	**Detects current sense voltage** 0: CS voltage < CS_VTH 1: CS voltage > CS_VTH
3	**RG_CS_E**	RG_CS_EN	**Enables current sense voltage detection comparator**

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Bit(s)	Mnemonic	Name	Description
	N		0: Disable 1: Enable
1	**RG_VBAT_CV_EN**	RG_VBAT_CV_EN	

0006 **CHR_CON3** **Charger Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**RG_VBAT_CV_VTH**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**RG_VBAT_CV_VTH**	RG_VBAT_CV_VTH	**Battery CV dection threshold trimming option** Default: 4.2V This register is used for FT CV threshold trimming and not for customer's fine-tuning (pchr_dig should invert MSB bit; otherwise, BC1.2 2.2V threshold will be wrong.) 0~7: 4.2000V (default), 125mV/step 8~12: 4.3250V, 250mV/step 13: 4.1625V 14: 4.1750V 15: 2.2V (BC1.2 application) 16: 4.0500V 17: 4.1000V 18: 4.1250V 19: 3.7750V 20: 3.8000V 21: 3.8500V 22: 3.9000V 23: 4.0000V 24: 4.0500V 25: 4.1000V 26: 4.1250V 27: 4.1375V 28: 4.1500V 29: 4.1625V 30: 4.1750V 31: 4.1875V

0008 **CHR_CON4** **Charger Control Register 4** **000F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RG_CS_VTH**			
Type													RW			
Reset													1	1	1	1

Bit(s)	Mnemonic	Name	Description
3:0	**RG_CS_VTH**	RG_CS_VTH	**Detects current sense voltage detection @ Rcs=0.2ohm** 0: 1600mA 1: 1500mA 2: 1400mA

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Bit(s)	Mnemonic	Name	Description
			3: 1300mA 4: 1200mA 5: 1100mA 6: 1000mA 7: 900mA 8: 800mA 9: 700mA 10: 650mA 11: 550mA 12: 450mA (USB download) 13: 300mA 14: 200mA 15: 70mA

000C **CHR_CON6** **Charger Control Register 6** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VBAT_OV_DET	RG_VBAT_OV_DEG		RG_VBAT_OV_VTH			RG_VBAT_OV_EN
Type										RO	RW		RW			RW
Reset										0	0		0	0	0	1

Bit(s)	Mnemonic	Name	Description
6	**VBAT_OV_DET**	RGS_VBAT_OV_DET	**Detects VBAT_OV voltage** 0: VBAT voltage < VBAT_OV_VTH 1: VBAT voltage > VBAT_OV_VTH
5	**RG_VBAT_OV_DEG**	RG_VBAT_OV_DEG	**Enables VBAT OV voltage detection deglitch** 0: No de-bounce 1: De-bounce one cycle (1us)
3:1	**RG_VBAT_OV_VTH**	RG_VBAT_OV_VTH	**Battery over-voltag detection threshold** 000: 4.200V (default) 001: 4.300V 010: 4.400V 011: 4.450V 1xx: 3.800V
0	**RG_VBAT_OV_EN**	RG_VBAT_OV_EN	**Enables VBAT OV over-voltage detection comparator**

000E **CHR_CON7** **Charger Control Register 7** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				RGS_BATON_UNDET										BATON_TDET_EN	RG_BATON_HT_EN	RG_BATON_EN
Type				RO										RW	RW	RW
Reset				0										0	0	1

Bit(s)	Mnemonic	Name	Description
12	**RGS_BAT**	RGS_BATON_U	**Detects BATON_UNDET voltage detection**

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Bit(s)	Mnemonic	Name	Description
	ON_UNDET	NDET	BATON_UNDET is always 0 during DDLO/UVLO. 0: Valid battery is detected. 1: Valid battery is not detected.
2	**BATON_TDET_EN**	BATON_TDET_EN	0: N/A 1: Enable BATON temperature detection
1	**RG_BATON_HT_EN**	RG_BATON_HT_EN	**Detects battery-on HW high temperature** 0: Disable 1: Enable
0	**RG_BATON_EN**	RG_BATON_EN	**Enables BATON_UNDET detection** 0: Disable comparator and BATON_UNDET = 0 1: Enable comparison

001A **CHR_CON13** **Charger Control Register 13** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**RG_CHRWDT_WR**				**RG_CHRWDT_EN**	**RG_CHRWDT_TD**			
Type								RW				RW	RW			
Reset								0				1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	**RG_CHRWDT_WR**	RG_CHRWDT_WR	**Resets charger watchdog timer and updates CHRWDT_TD** 0: Reset inactive 1: Reset active and CHRWDT_TD is updated to PCHR_DIG.
4	**RG_CHRWDT_EN**	RG_CHRWDT_EN	**Enabling setting for charger watchdog timer** 0: Disable 1: Enable if (CHR_EN(@CHR_CON0) == 1) *Note:* *1. UVLO does not care this bit and will time out after 3,000s.* *2. PCHR_TESTMODE can force to control watchdog enabling by using this bit.*
3:0	**RG_CHRWDT_TD**	RG_CHRWDT_TD	**Time constant setting for charger watchdog timer** 0: 4 sec 1: 8 sec 2: 16 sec 3: 32 sec 4: 128 sec 5: 256 sec 6: 512 sec 7: 1,024 sec 8~15: 3,000 sec

001E **CHR_CON15** **Charger Control Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**RGS_CHRWDT_OUT**	**RG_CHRWDT_FLAG_WR**	**RG_CHRWDT_INT_EN**

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Type														RO	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**RGS_CHRWDT_OUT**	RGS_CHRWDT_OUT	**Time-out flag for charger watchdog timer** Read: 0: No time-out status 1: Time-out status is asserted.
1	**RG_CHRWDT_FLAG_WR**	RG_CHRWDT_FLAG_WR	**Clear time-out flag for charger watchdog timer** Read: 0: N/A (while RGS_CHRWDT_OUT = 0) 1: Clear time-out flag while RGS_CHRWDT_OUT = 1
0	**RG_CHRWDT_INT_EN**	RG_CHRWDT_INT_EN	**Interrupt enabling setting for charger watchdog timer** 0: Disable 1: Enable

0020 CHR_CON16 Charger Control Register 16 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_USBDL_SET	RG_USBDL_RST	RG_UVLO_VTHL	
Type													RW	RW	RW	
Reset													0	0	0	1

Bit(s)	Mnemonic	Name	Description
3	**RG_USBDL_SET**	RG_USBDL_SET	**USBDL_MODE software set control** 0: No effect 1: Force to enter USBDL MODE
2	**RG_USBDL_RST**	RG_USBDL_RST	**USBDL_MODE software reset control** 0: No effect 1: Force to leave USBDL MODE (priority is less than USBDL_DET)
1:0	**RG_UVLO_VTHL**	RG_UVLO_VTHL	**Selects UVLO low threshold** 0: 2.9V 1: 2.75V (default) 2: 2.6V 3: 2.5V

0022 CHR_CON17 Charger Control Register 17 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_BGR_UNCHOP	RG_BGR_UNCHOP_PH		RG_BGR_RSEL		
Type											RW	RW		RW		
Reset											0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
5	**RG_BGR_**	RG_BGR_UNCH	**BGR unchop mode**

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Bit(s)	Mnemonic	Name	Description
	UNCHOP	OP	0: Chop mode 1: Unchop mode
4	**RG_BGR_UNCHOP_PH**	RG_BGR_UNCHOP_PH	**Selects BGR unchop mode phase** 0: Select phase 0 path in the unchop mode. 1: Select phase 1 path in the unchop mode.
2:0	**RG_BGR_RSEL**	RG_BGR_RSEL	**Selects BGR resistor (R0 = R1), R2=85K, and VBG=(R0/R2)*dVBE+VBE** 0: c0, 780K (default) 1: c1, 820K 2: c2, 860K 3: c3, 900K 4: cm4, 620K 5: cm3, 660K 6: cm2, 700K 7: cm1, 740K

0024 **CHR_CON18** **Charger Control Register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_BC11_CMP_OUT				RG_BC11_VSRC_EN		RG_BC11_RST	RG_BC11_BB_CTRL
Type									RO				RW		RW	RW
Reset									0				0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**RGS_BC11_CMP_OUT**	RGS_BC11_CMP_OUT	**Comparison result of BC11 charger detection** 0: DP or DM < BC11_VREF_VTH 1: DP or DM > BC11_VREF_VTH
3:2	**RG_BC11_VSRC_EN**	RG_BC11_VSRC_EN	**BC11 voltage source** Set VDP_SRC = 0.6V 0: Disable the voltage 1: Enable the voltage source to DM 2: Enable the voltage source to DP 3: Forbidden
1	**RG_BC11_RST**	RG_BC11_RST	**Resets BC11 detection mechanism in PCHR_DIG** 0: No effect 1: BC11 detection mechanism is disabled in PCHR_DIG.
0	**RG_BC11_BB_CTRL**	RG_BC11_BB_CTRL	**Forces BC11 charger detection to be controlled by baseband** 0: BC11 detection by PCHR_DIG (hardware mode) 1: BC11 detection by baseband (software mode)

0026 **CHR_CON19** **Charger Control Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_BC11_BIAS_EN	RG_BC11_IPU_EN		RG_BC11_IPD_EN		RG_BC11_CMP_EN		RG_BC11_VREF_VTH	
Type								RW	RW		RW		RW		RW	
Reset								0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
8	**RG_BC11_BIAS_EN**	RG_BC11_BIAS_EN	**Enables BC11 detection bias circuit** 0: Disable 1: Enable
7:6	**RG_BC11_IPU_EN**	RG_BC11_IPU_EN	**Enables BC11 7~15uA pull-up current** 0: Disable pull-up current 1: Enable pull-up current to DM 2: Enable pull-up current to DP 3: Forbidden
5:4	**RG_BC11_IPD_EN**	RG_BC11_IPD_EN	**BC11 50~150uA pull-down current** 0: Disable pull-down current 1: Enable pull-down current to DM 2: Enable pull-down current to DP 3: Forbidden
3:2	**RG_BC11_CMP_EN**	RG_BC11_CMP_EN	**BC11 comparator connection** 0: Disable comparator 1: Enable comparator to DM 2: Enable comparator to DP 3: Forbidden
1:0	**RG_BC11_VREF_VTH**	RG_BC11_VREF_VTH	**VREF threshold voltage for comparator** 0: VREF_VTH = 0.325V 1: VREF_VTH = 1.2V 2, 3: VREF_VTH = 2.6V (for Apple adaptor)

002C **CHR_CON22** **Charger Control Register 22** **0044**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RG_CHRIND_DIMMING**	**RG_CHRIND_ON**	**RG_LOW_ICH_DB**					
Type									RW	RW	RW					
Reset									0	1	0	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
7	**RG_CHRIND_DIMMING**	RG_CHRIND_DIMMING	**Enables pre-charge indicator dimming** 0: Disable 1: Enable
6	**RG_CHRIND_ON**	RG_CHRIND_ON	**Pre-charge indicator on** 0: Disable 1: Enable
5:0	**RG_LOW_ICH_DB**	RG_LOW_ICH_DB	**Plug out HW detection de-bounce time (base = 16ms)** De-bounce time: RG_LOW_ICH_DB x 16ms

002E **CHR_CON23** **Charger Control Register 23** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RG_ULC_D**	**RG_HWCV**		**RG_TRAC**		**RG_CSDAC**		

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									ET_EN	_EN		KING_EN		_MODE		
Type									RW	RW		RW		RW		
Reset									0	0		1		0		

Bit(s)	Mnemonic	Name	Description
7	**RG_ULC_DET_EN**	RG_ULC_DET_EN	**Enables charger plug-out auto detection** This fuction must be applied with RG_HWCV_EN = 1. 0: Disable 1: Enable
6	**RG_HWCV_EN**	RG_HWCV_EN	**Enables hardware CV current tracking** 0: Disable 1: Enable
4	**RG_TRACKING_EN**	RG_TRACKING_EN	1: Enable HTH/LTH for current tracking 0: N/A 1: Enable
2	**RG_CSDAC_MODE**	RG_CSDAC_MODE	0: If not entering CC, charging is AUTO mode 1: If leaving UVLO, charging is controlled by RG_CSDAC_EN (same as CC mode).

0036 CHR_CON27 Charger Control Register 27 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_BGR_TEST_RSTB	RG_BGR_TEST_EN	QI_BGR_EXT_BUF_EN					
Type									RW	RW	RW					
Reset									0	0	0					

Bit(s)	Mnemonic	Name	Description
7	**RG_BGR_TEST_RSTB**	RG_BGR_TEST_RSTB	**Bandgap reference FT test mode resetb signal (also gated by RG_BGR_TEST_EN=0 & PMU_TESTMODE=0) -> GPIO control in test mode** 0: Reset 1: Does not reset
6	**RG_BGR_TEST_EN**	RG_BGR_TEST_EN	**Bandgap reference FT test mode enabling signal** 0: Normal mode 1: Test mode (should combine PMU_TESTMODE=1)
5	**QI_BGR_EXT_BUF_EN**	QI_BGR_EXT_BUF_EN	**Bandgap reference buffer for external use (MT8320)** 0: Disable 1: Enable (default)

0038 CHR_CON28 Charger Control Register 28 0055

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DAC_USBDL_MAX									
Type							RW									
Reset							0	0	0	1	0	1	0	1	0	1

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Bit(s)	Mnemonic	Name	Description
9:0	**RG_DAC_USBDL_MAX**	RG_DAC_USBDL_MAX	**CS DAC maximum limit** When in USB download mode, CS DAC value is limited by this setting. Default: 450mA

003C STRUP_CON0 STRUP Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											THR_HWPDN_EN					THR_DET_DIS
Type											RW					RW
Reset											0					0

Bit(s)	Mnemonic	Name	Description
5	**THR_HWPDN_EN**	THR_HWPDN_EN	**Enables theraml auto power-down** 0: Disable 1: Enable
0	**THR_DET_DIS**	THR_DET_DIS	**Disables thermal detection function** 0: Normal mode 1: Disable thermal detection

003E STRUP_CON2 STRUP Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_STRUP_IREF_TRIM				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	**RG_STRUP_IREF_TRIM**	RG_STRUP_IREF_TRIM	**Reference current trimming bits** Trimmming current range: 0.5uA ~ 1.4375uA (step = 31.25nA), typ = 1uA 00000: 1uA 00001~01111: +31.25nA/step 10000: 0.5uA 10001~11111: -31.25nA/step

0040 STRUP_CON3 STRUP Control Register 3 4001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VREF_BG												RG_FCHR_PU_EN	RG_FCHR_KEYDET_EN	
Type		RW												RW	RW	
Reset		1	0	0										0	0	

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Bit(s)	Mnemonic	Name	Description
14:12	**RG_VREF_BG**	RG_VREF_BG	**Reference current fine tunning to compensate bandgap (BG) voltage variation** 000: VBG=1.16V 001: VBG=1.17V 010: VBG=1.18V 011: VBG=1.19V 100: VBG=1.20V 101: VBG=1.21V 110: VBG=1.22V 111: VBG=1.23V
2	**RG_FCHR_PU_EN**	RG_FCHR_PU_EN	**Enables FCHR internal resistor pull-up** 0: Disable pull up R 1: Enable pull up R
1	**RG_FCHR_KEYDET_EN**	RG_FCHR_KEYDET_EN	**FCHR mode state hold without key press detection feature** 0: Disable 1: Enable

0044 **STRUP_CON5** **STRUP Control Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**PMU_THR_STATUS**										
Type						RO										
Reset						0	0	0								

Bit(s)	Mnemonic	Name	Description
10:8	**PMU_THR_STATUS**	PMU_THR_STATUS	Thermal detection status

004A **STRUP_CON8** **STRUP Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_OSC_EN**	**JUST_PWRKEY_RST**														
Type	RO	RO														
Reset	0	0														

Bit(s)	Mnemonic	Name	Description
15	**QI_OSC_EN**	QI_OSC_EN	**Enables internal oscillaotr** 0: Disable 1: Enable
14	**JUST_PWRKEY_RST**	JUST_PWRKEY_RST	**Long pressed reset indicator**

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004C STRUP_CON9 STRUP Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															STRUP_EXT_PMIC_SEL	STRUP_EXT_PMIC_EN
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**STRUP_EXT_PMIC_SEL**	STRUP_EXT_PMIC_SEL	**Selects QI_EXT_PMIC_EN control** 0: HW mode 1: SW mode
0	**STRUP_EXT_PMIC_EN**	STRUP_EXT_PMIC_EN	**Enables QI_EXT_PMIC_EN software mode**

004E STRUP_CON10 STRUP Control Register 10 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									STRUP_AUXADC_RSTB_SEL	STRUP_AUXADC_START_SEL	STRUP_AUXADC_RSTB_SW	STRUP_AUXADC_START_SW				
Type									RW	RW	RW	RW				
Reset									0	0	0	0				

Bit(s)	Mnemonic	Name	Description
7		STRUP_AUXADC_RSTB_SEL	**Selects STRUP_AUXADC_RSTB** 0: HW mode 1: SW mode
6		STRUP_AUXADC_START_SEL	**Selects STRUP_AUXADC_START** 0: HW mode 1: SW mode
5		STRUP_AUXADC_RSTB_SW	**STRUP_AUXADC_RSTB SW path**
4		STRUP_AUXADC_START_SW	**STRUP_AUXADC_START SW path**

0052 SPK_CON0 Speaker Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SPK_THER_SHDN_L_EN	SPK_OC_SHDN_DL						SPKMODE_L		SPK_EN_L
Type							RW	RW						RW		RW
Reset							0	0						0		0

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Bit(s)	Mnemonic	Name	Description
9	**SPK_THER_SHDN_L_EN**	SPK_THER_SHDN_L_EN	**Enables speaker L-ch thermal shut-down** 0: Disable 1: Enable
8	**SPK_OC_SHDN_DL**	SPK_OC_SHDN_DL	**Shuts down class D mode L-ch OC event** 0: Normal 1: Shut-down (turn off SPK output stage)
2	**SPKMODE_L**	SPKMODE_L	**Selects speaker L-ch driver mode** 0: Class D mode 1: Class AB mode
0	**SPK_EN_L**	SPK_EN_L	**Enables speaker amp. L-ch** 0: Disable 1: Enable

0056 **SPK_CON2** **Speaker Control Register 2** **0014**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**RG_SPK_OC_EN_L**	**RG_SPKAB_OC_EN_L**			**RG_SPKRCV_EN_L**			**RG_SPK_SLEW_L**			**RG_SPK_INTG_RST_L**
Type						RW	RW			RW			RW			RW
Reset						0	0			0			0	1		0

Bit(s)	Mnemonic	Name	Description
10	**RG_SPK_OC_EN_L**	RG_SPK_OC_EN_L	**Enables class D L-ch over-current protection** 0: Disable 1: Enable
9	**RG_SPKAB_OC_EN_L**	RG_SPKAB_OC_EN_L	**Enables class AB mode L-ch over-current protection**
6	**RG_SPKRCV_EN_L**	RG_SPKRCV_EN_L	**Enables speaker L-ch receiver mode voice bypass** 0: Disable 1: Enable
3:2	**RG_SPK_SLEW_L**	RG_SPK_SLEW_L	**Controls class D L-ch slew rate** 00: 3/4, 10.8n /8.3n (rise/fall) 01: 4/4, 8.8n /6.3n 10: 1/4, 16.4n /15n 11: 2/4, 13.8n/12.6n
0	**RG_SPK_INTG_RST_L**	RG_SPK_INTG_RST_L	**Controls speaker L-ch integrator reset** 0: No reset 1: Reset on

005E **SPK_CON6** **Speaker Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPK_AB_OC_L**	**SPK_D_OC_L_**			**SPK_OC_THD**		**SPK_OC_WND**									

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	_DEG	DEG														
Type	RO	RO			RW		RW									
Reset	0	0			0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15	**SPK_AB_OC_L_DEG**	SPK_AB_OC_L_DEG	**Class AB L-ch OC flag with deglitch**
14	**SPK_D_OC_L_DEG**	SPK_D_OC_L_DEG	**Class D L-ch OC flag with deglitch**
11:10	**SPK_OC_THD**	SPK_OC_THD	**Threshold setting in the decision window for SPK over-current status** 0: 4/8 1: 3/8 2: 2/8 3: 1/8
9:8	**SPK_OC_WND**	SPK_OC_WND	**Decision window setting for SPK over-current status** 0: 16us 1: 32us 2: 64us 3: 128us

0062 SPK_CON8 Speaker Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_SPK_CCODE							
Type									RW							
Reset									0	0	0	0				

Bit(s)	Mnemonic	Name	Description
7:4	**RG_SPK_CCODE**	RG_SPK_CCODE	**Class D modulation frequency control code** x000: 288k x001: 418.8k x010: 541k x011: 656k x100: 766k x101: 966k x110: 1.148M x111: 1.646M

0064 SPK_CON9 Speaker Control Register 9 2000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_SPKPGA_GAIN											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11:8	**RG_SPKPGA_GAIN**	RG_SPKPGA_GAIN	**Speaker PGA gain control** 0000: Mute 0001: 0dB 0010: 4dB

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Bit(s)	Mnemonic	Name	Description
			0011: 5dB 0100: 6dB 0101: 7dB 0110: 8dB 0111: 9dB 1000: 10dB 1001: 11dB 1010: 12dB 1011: 13dB 1100: 14dB 1101: 15dB 1110: 16dB 1111: 17dB

006A **SPK_CON12** **Speaker Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SPK_OUTSTG_EN_L_SW		SPK_EN_L_SW		SPK_DEPOP_EN_L_SW		SPKMODE_L_SW		SPK_RST_L_SW			
Type					RW		RW		RW		RW		RW			
Reset					0		0		0		0		0			

Bit(s)	Mnemonic	Name	Description
11	**SPK_OUTSTG_EN_L_SW**	SPK_OUTSTG_EN_L_SW	**Spekaer left channel output stage enabling control**
9	**SPK_EN_L_SW**	SPK_EN_L_SW	**Enables speaker amp. L-ch** 0: Disable 1: Enable
7	**SPK_DEPOP_EN_L_SW**	SPK_DEPOP_EN_L_SW	**Class D L-ch mode depop enabling flag**
5	**SPKMODE_L_SW**	SPKMODE_L_SW	**Selects speaker L-ch driver mode** 0: Class D mode 1: Class AB mode
3	**SPK_RST_L_SW**	SPK_RST_L_SW	**Resets class D L-ch** 0: Normal 1: Reset

011A **TOP_RST_MISC** **Reset Control Misc** **0011**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_PWRKEY_RST_TD		RG_PWRRST_TMR_DIS	RG_PWRKEY_RST_EN	RG_HOMEKEY_RST_EN	RG_RST_PART_SEL		RG_STRUP_MAN_RST_EN	RG_SYSRSTB_EN	RG_AP_RST_DIS
Type							RW		RW	RW	RW	RW		RW	RW	RW
Reset							0	0	0	0	0	1		0	0	1

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Bit(s)	Mnemonic	Name	Description
9:8	**RG_PWRKEY_RST_TD**	RG_PWRKEY_RST_TD	**Resets PWRKEY long pressed time to issue** 2'b00: 8 sec 2'b01: 11 sec 2'b10: 14 sec 2'b11: 5 sec
7	**RG_PWRRST_TMR_DIS**	RG_PWRRST_TMR_DIS	**Enables/Disables PWRKEY long pressed timer** 1'b0: 1-> 0 enable timer 1'b1: 0-> 1 disable timer
6	**RG_PWRKEY_RST_EN**	RG_PWRKEY_RST_EN	**Enables PWRKEY long pressed reset** 1'b1: Enable reset 1'b0: Disable reset
5	**RG_HOMEKEY_RST_EN**	RG_HOMEKEY_RST_EN	**Enables RSTKEY long pressed reset** 1'b1: Enable reset 1'b0: Disable reset
4	**RG_RST_PART_SEL**	RG_RST_PART_SEL	**Disables SYSRSTB reset PCHR_DIG** 1'b1: Enable reset 1'b0: Disable reset
2	**RG_STRUP_MAN_RST_EN**	RG_STRUP_MAN_RST_EN	**Enables STRUP circuit manual reset** 1'b0: Disable manual reset 1'b1: Enable manual reset
1	**RG_SYSRSTB_EN**	RG_SYSRSTB_EN	**SYSRSTB (external watchdog) reset from AP** 1'b0: Disable 1'b1: Enable
0	**RG_AP_RST_DIS**	RG_AP_RST_DIS	**Asserts ap power-on reset once external reset state 2 happens** 1'b0: Enable 1'b1: Disable

0132 **TEST_OUT** **TEST_OUT** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TEST_OUT			
Type													RO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**TEST_OUT**	TEST_OUT	Monitoring

0142 **CHRSTATUS** **CHR Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RO_BATON_UNDET	PCHR_CHRDET	VBAT_OV	FCHRKEY_DEB	PWRKEY_DEB	
Type											RO	RO	RO	RO	RO	
Reset											0	0	0	0	0	

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Bit(s)	Mnemonic	Name	Description
5		RO_BATON_UNDET	
4	**PCHR_CHRDET**	PCHR_CHRDET	
3	**VBAT_OV**	VBAT_OV	
2	**FCHRKEY_DEB**	FCHRKEY_DEB	
1	**PWRKEY_DEB**	PWRKEY_DEB	

0144 TDSEL_CON TDSEL_CON 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_SIMLS_TDSEL		RG_PMU_TDSEL	RG_SPI_TDSEL	RG_AUD_TDSEL	RG_SIMAP_TDSEL
Type											RW		RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:4	**RG_SIMLS_TDSEL**	RG_SIMLS_TDSEL	TDSEL
3	**RG_PMU_TDSEL**	RG_PMU_TDSEL	TDSEL
2	**RG_SPI_TDSEL**	RG_SPI_TDSEL	TDSEL
1	**RG_AUD_TDSEL**	RG_AUD_TDSEL	TDSEL
0	**RG_SIMAP_TDSEL**	RG_SIMAP_TDSEL	TDSEL

0146 RDSEL_CON RDSEL_CON 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_SIMLS_RDSEL		RG_PMU_RDSEL	RG_SPI_RDSEL	RG_AUD_RDSEL	RG_SIMAP_RDSEL
Type											RW		RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:4	**RG_SIMLS_RDSEL**	RG_SIMLS_RDSEL	RDSEL
3	**RG_PMU_RDSEL**	RG_PMU_RDSEL	RDSEL
2	**RG_SPI_RDSEL**	RG_SPI_RDSEL	RDSEL

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Bit(s)	Mnemonic	Name	Description
1	**RG_AUD_RDSEL**	RG_AUD_RDSEL	RDSEL
0	**RG_SIMAP_RDSEL**	RG_SIMAP_RDSEL	RDSEL

0148 **SMT_CON0** **SMT_CON0** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RG_SMT_RTC_32K1V8**	**RG_SMT_SRCLKEN**	**RG_SMT_INT**	**RG_SMT_SYSRSTB**
Type													RW	RW	RW	RW
Reset													0	1	0	0

Bit(s)	Mnemonic	Name	Description
3	**RG_SMT_RTC_32K1V8**	RG_SMT_RTC_32K1V8	**SMT** 0: Disable 1: Enable
2	**RG_SMT_SRCLKEN**	RG_SMT_SRCLKEN	**SMT** 0: Disable 1: Enable
1	**RG_SMT_INT**	RG_SMT_INT	**SMT** 0: Disable 1: Enable
0	**RG_SMT_SYSRSTB**	RG_SMT_SYSRSTB	**SMT** 0: Disable 1: Enable

014A **SMT_CON1** **SMT_CON1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**RG_SMT_SPI_MISO**	**RG_SMT_SPI_MOSI**	**RG_SMT_SPI_CSN**	**RG_SMT_SPI_CLK**
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3	**RG_SMT_SPI_MISO**	RG_SMT_SPI_MISO	**SMT** 0: Disable 1: Enable
2	**RG_SMT_SPI_MOSI**	RG_SMT_SPI_MOSI	**SMT** 0: Disable 1: Enable
1	**RG_SMT_SPI_CSN**	RG_SMT_SPI_CSN	**SMT** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
0	**RG_SMT_SPI_CLK**	RG_SMT_SPI_CLK	**SMT** 0: Disable 1: Enable

014C SMT_CON2 SMT_CON2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_SMT_AUD_MISO	RG_SMT_AUD_MOSI	RG_SMT_AUD_CLK
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	**RG_SMT_AUD_MISO**	RG_SMT_AUD_MISO	**SMT** 0: Disable 1: Enable
1	**RG_SMT_AUD_MOSI**	RG_SMT_AUD_MOSI	**SMT** 0: Disable 1: Enable
0	**RG_SMT_AUD_CLK**	RG_SMT_AUD_CLK	**SMT** 0: Disable 1: Enable

014E SMT_CON3 SMT_CON3 000C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_SMT_SIMLS1_SRST	RG_SMT_SIMLS1_SCLK	RG_SMT_SIM1_AP_SRST	RG_SMT_SIM1_AP_SCLK
Type													RW	RW	RW	RW
Reset													1	1	0	0

Bit(s)	Mnemonic	Name	Description
3	**RG_SMT_SIMLS1_SRST**	RG_SMT_SIMLS1_SRST	**SMT** 0: Disable 1: Enable
2	**RG_SMT_SIMLS1_SCLK**	RG_SMT_SIMLS1_SCLK	**SMT** 0: Disable 1: Enable
1	**RG_SMT_SIM1_AP_SRST**	RG_SMT_SIM1_AP_SRST	**SMT** 0: Disable 1: Enable
0	**RG_SMT_SIM1_AP_SCLK**	RG_SMT_SIM1_AP_SCLK	**SMT** 0: Disable 1: Enable

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0150 SMT_CON4 SMT_CON4 000C

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_SMT_SIMLS2_SRST	RG_SMT_SIMLS2_SCLK	RG_SMT_SIM2_AP_SRST	RG_SMT_SIM2_AP_SCLK
Type													RW	RW	RW	RW
Reset													1	1	0	0

Bit(s)	Mnemonic	Name	Description
3	**RG_SMT_SIMLS2_SRST**	RG_SMT_SIMLS2_SRST	**SMT** 0: Disable 1: Enable
2	**RG_SMT_SIMLS2_SCLK**	RG_SMT_SIMLS2_SCLK	**SMT** 0: Disable 1: Enable
1	**RG_SMT_SIM2_AP_SRST**	RG_SMT_SIM2_AP_SRST	**SMT** 0: Disable 1: Enable
0	**RG_SMT_SIM2_AP_SCLK**	RG_SMT_SIM2_AP_SCLK	**SMT** 0: Disable 1: Enable

0152 DRV_CON0 DRV_CON0 0CCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_OCTL_RTC_32K1V8				RG_OCTL_SRCLKEN				RG_OCTL_INT			
Type					RW				RW				RW			
Reset					1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
11:8	**RG_OCTL_RTC_32K1V8**	RG_OCTL_RTC_32K1V8	OC CTL
7:4	**RG_OCTL_SRCLKEN**	RG_OCTL_SRCLKEN	OC CTL
3:0	**RG_OCTL_INT**	RG_OCTL_INT	OC CTL

0154 DRV_CON1 DRV_CON1 CCCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_SPI_MISO				RG_OCTL_SPI_MOSI				RG_OCTL_SPI_CSN				RG_OCTL_SPI_CLK			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
15:12	**RG_OCTL_SPI_MISO**	RG_OCTL_SPI_MISO	OC CTL
11:8	**RG_OCTL_SPI_MOSI**	RG_OCTL_SPI_MOSI	OC CTL
7:4	**RG_OCTL_SPI_CSN**	RG_OCTL_SPI_CSN	OC CTL
3:0	**RG_OCTL_SPI_CLK**	RG_OCTL_SPI_CLK	OC CTL

0156 DRV_CON2 DRV_CON2 0CCC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_OCTL_AUD_MISO				RG_OCTL_AUD_MOSI				RG_OCTL_AUD_CLK			
Type					RW				RW				RW			
Reset					1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
11:8	**RG_OCTL_AUD_MISO**	RG_OCTL_AUD_MISO	OC CTL
7:4	**RG_OCTL_AUD_MOSI**	RG_OCTL_AUD_MOSI	OC CTL
3:0	**RG_OCTL_AUD_CLK**	RG_OCTL_AUD_CLK	OC CTL

0158 DRV_CON3 DRV_CON3 22CC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_SIMLS1_SRST				RG_OCTL_SIMLS1_SCLK				RG_OCTL_SIM1_AP_SRST				RG_OCTL_SIM1_AP_SCLK			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	0	1	0	1	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
15:12	**RG_OCTL_SIMLS1_SRST**	RG_OCTL_SIMLS1_SRST	OC CTL
11:8	**RG_OCTL_SIMLS1_SCLK**	RG_OCTL_SIMLS1_SCLK	OC CTL
7:4	**RG_OCTL_SIM1_AP_SRST**	RG_OCTL_SIM1_AP_SRST	OC CTL
3:0	**RG_OCTL_SIM1_AP_SCLK**	RG_OCTL_SIM1_AP_SCLK	OC CTL

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015A DRV_CON4 DRV_CON4 22CC

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_SIMLS2_SRST				RG_OCTL_SIMLS2_SCLK				RG_OCTL_SIM2_AP_SRST				RG_OCTL_SIM2_AP_SCLK			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	0	1	0	1	1	0	0	1	1	0	0

Bit(s)	Mnemonic	Name	Description
15:12	**RG_OCTL_SIMLS2_SRST**	RG_OCTL_SIMLS2_SRST	OC CTL
11:8	**RG_OCTL_SIMLS2_SCLK**	RG_OCTL_SIMLS2_SCLK	OC CTL
7:4	**RG_OCTL_SIM2_AP_SRST**	RG_OCTL_SIM2_AP_SRST	OC CTL
3:0	**RG_OCTL_SIM2_AP_SCLK**	RG_OCTL_SIM2_AP_SCLK	OC CTL

015C SIMLS1_CON SIMLS1_CON 0033

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_SIMLS1_SRST_CONF				RG_SIMLS1_SCLK_CONF			
Type									RW				RW			
Reset									0	0	1	1	0	0	1	1

Bit(s)	Mnemonic	Name	Description
7:4	**RG_SIMLS1_SRST_CONF**	RG_SIMLS1_SRST_CONF	**SIM CONF** 0: SR0 1: SR1 2: R0 3: R1
3:0	**RG_SIMLS1_SCLK_CONF**	RG_SIMLS1_SCLK_CONF	**SIM CONF** 0: SR0 1: SR1 2: R0 3: R1

015E SIMLS2_CON SIMLS2_CON 0033

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_SIMLS2_SRST_CONF				RG_SIMLS2_SCLK_CONF			
Type									RW				RW			
Reset									0	0	1	1	0	0	1	1

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Bit(s)	Mnemonic	Name	Description
7:4	**RG_SIMLS2_SRST_CONF**	RG_SIMLS2_SRST_CONF	**SIM CONF** 0: SR0 1: SR1 2: R0 3: R1
3:0	**RG_SIMLS2_SCLK_CONF**	RG_SIMLS2_SCLK_CONF	**SIM CONF** 0: SR0 1: SR1 2: R0 3: R1

0182 FQMTR_CON0 Frequency Meter Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQMTR_EN												FQMTR_BUSY	FQMTR_TCKSEL		
Type	RW												RO	RW		
Reset	0												0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**FQMTR_EN**	FQMTR_EN	**Enables frequency meter** 0: Disable 1: Enable
3	**FQMTR_BUSY**	FQMTR_BUSY	**Frequency meter busy status** 0: Ready 1: Busy
2:0	**FQMTR_TCKSEL**	FQMTR_TCKSEL	**Selects frequency meter target (measured) clock**

0184 FQMTR_CON1 Frequency Meter Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQMTR_WINSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**FQMTR_WINSET**	FQMTR_WINSET	Frequency meter window setting (= numbers of FIXED clock cycles)

0186 FQMTR_CON2 Frequency Meter Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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0186 **FQMTR_CON 2** **Frequency Meter Control Register 2** **0000**

Name	FQMTR_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**FQMTR_DATA**	FQMTR_DATA	Frequency meter data to be read out

0188 **RG_SPI_CON** **SPI Control Register** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_SPI_CON
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**RG_SPI_CON**	RG_SPI_CON	**Selects analog SW channel** 0: Channel 1 1: Channel 2

018A **DEW_DIO_EN** **Dual I/O Mode Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEW_DIO_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DEW_DIO_EN**	DEW_DIO_EN	**Enables/Disables dual I/O mode for SPI slave** It is effective immediately after being set. Therefore there should be a guard band with no SPI transaction when dual I/O mode is toggled. 0: Disable dual I/O mode 1: Enable dual I/O mode

018C **DEW_READ_TEST** **Read Test** **5AA5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEW_READ_TEST															
Type	RO															
Reset	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1

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Bit(s)	Mnemonic	Name	Description
15:0	**DEW_READ_TEST**	DEW_READ_TEST	**Dummy register used to test read access** Read this register to check if it matches the default value. The read test should be prior to the write test.

018E **DEW_WRITE_TEST** **Write Test** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DEW_WRITE_TEST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**DEW_WRITE_TEST**	DEW_WRITE_TEST	**Dummy register used to test write access** It is not related to any hardware function circuit except for regiter read/write. Write to this register and read back to check if they match. The read test should be prior to the write test.

0190 **DEW_CRC_SWRST** **CRC_SWRST** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEW_CRC_SWRST
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DEW_CRC_SWRST**	DEW_CRC_SWRST	Set to 1 to reset CRC calculation circuit.

0192 **DEW_CRC_EN** **CRC Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEW_CRC_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
0	**DEW_CRC_EN**	DEW_CRC_EN	Set to 1 to enable CRC calculation circuit.

0194 **DEW_CRC_VAL** **CRC Value** **0083**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DEW_CRC_VAL							
Type									RO							
Reset									1	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
7:0	**DEW_CRC_VAL**	DEW_CRC_VAL	Current CRC value

0196 **DEW_DBG_MON_SEL** **Monitor Flag Group Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													DEW_DBG_MON_SEL			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**DEW_DBG_MON_SEL**	DEW_DBG_MON_SEL	Selects monitor flag group for PMIC_DEWRAP

0198 **DEW_CIPHER_KEY_SEL** **CIPHER Key Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															DEW_CIPHER_KEY_SEL	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**DEW_CIPHER_KEY_SEL**	DEW_CIPHER_KEY_SEL	**Selects CIPHER key** All keys are hard-wired.

019A **DEW_CIPHER_IV_SEL** **CIPHER Initial Vector Selection** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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019A	DEW_CIPHER_IV_SEL	CIPHER Initial Vector Selection	0000

Name															DEW_CIPHER_IV_SEL	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**DEW_CIPHER_IV_SEL**	DEW_CIPHER_IV_SEL	**Selects CIPHER initial vector** Set to 0 to choose manual initial vector; otherwise, choose other hard-wired initial vectors.

019C	DEW_CIPHER_EN	CIPHER Engine Enable	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEW_CIPHER_EN
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DEW_CIPHER_EN**	DEW_CIPHER_EN	Starts CIPHER engine

019E	DEW_CIPHER_RDY	CIPHER Data Ready	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEW_CIPHER_RDY
Type																RO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DEW_CIPHER_RDY**	DEW_CIPHER_RDY	**CIPHER data ready** The data should be ready before enabling CIPHER_MODE.

01A0	DEW_CIPHER_MODE	CIPHER Mode Enable	0000

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01A0 **DEW_CIPHER_MODE** **CIPHER Mode Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DEW_CIPHER_MODE**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DEW_CIPHER_MODE**	DEW_CIPHER_MODE	**Enablse CIPHER mode** 0: Disable 1: Enable

01A2 **DEW_CIPHER_SWRST** **CIPHER Soft Reset** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DEW_CIPHER_SWRST**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DEW_CIPHER_SWRST**	DEW_CIPHER_SWRST	CIPHER soft reset

01A4 **DEW_RDDMY_NO** **Read Dummy Cycle Number** **000F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**DEW_RDDMY_NO**			
Type													RW			
Reset													1	1	1	1

Bit(s)	Mnemonic	Name	Description
3:0	**DEW_RDDMY_NO**	DEW_RDDMY_NO	Apply (1+RDDMY[3:0])T of dummy read cycles before read data phase. This setting should be in accordance with the one in master.

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01A6	DEW_RDATA_DLY_SEL	Read Data Delay Configuration	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																DEW_RDATA_DLY_SEL
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**DEW_RDATA_DLY_SEL**	DEW_RDATA_DLY_SEL	**Allows user to choose latching time of read data from PMIC registers in different clock domains to prevent meta stability problems.** 0: No delay 1: Delay 1T of register clock

021E	VPROC_CON9	VPROC Control Register 9	0048

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VPROC_VOSEL						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0	**VPROC_VOSEL**	VPROC_VOSEL	**Selects VOUT in register mode** 0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V

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Bit(s)	Mnemonic	Name	Description
			0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V

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Bit(s)	Mnemonic	Name	Description
			1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0304 VPA_CON2 VPA Control Register 2 0200

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_VPA_MODESET								
Type								RW								
Reset								0								

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
8	**RG_VPA_MODESET**	RG_VPA_MODESET	1: Force PWM mode 0: Auto mode

030E **VPA_CON7** **VPA Control Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**QI_VPA_EN**													**VPA_EN**
Type			RO													RW
Reset			0													0

Bit(s)	Mnemonic	Name	Description
13	**QI_VPA_EN**	QI_VPA_EN	**Enables signal** 0: Disable 1: Enable
0	**VPA_EN**	VPA_EN	**Enable** 0: Disable 1: Enable

0312 **VPA_CON9** **VPA Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**VPA_VOSEL**					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0	**VPA_VOSEL**	VPA_VOSEL	**Selects VOUT in register mode** 000000: 0.50V 000001: 0.55V 000010: 0.60V 000011: 0.65V 000100: 0.70V 000101: 0.75V 000110: 0.80V 000111: 0.85V 001000: 0.90V 001001: 0.95V 001010: 1.00V 001011: 1.05V 001100: 1.10V 001101: 1.15V 001110: 1.20V 001111: 1.25V 010000: 1.30V 010001: 1.35V 010010: 1.40V 010011: 1.45V 010100: 1.50V 010101: 1.55V

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Bit(s)	Mnemonic	Name	Description
			010110: 1.60V 010111: 1.65V 011000: 1.70V 011001: 1.75V 011010: 1.80V 011011: 1.85V 011100: 1.90V 011101: 1.95V 011110: 2.00V 011111: 2.05V 100000: 2.10V 100001: 2.15V 100010: 2.20V 100011: 2.25V 100100: 2.30V 100101: 2.35V 100110: 2.40V 100111: 2.45V 101000: 2.50V 101001: 2.55V 101010: 2.60V 101011: 2.65V 101100: 2.70V 101101: 2.75V 101110: 2.80V 101111: 2.85V 110000: 2.90V 110001: 2.95V 110010: 3.00V 110011: 3.05V 110100: 3.10V 110101: 3.15V 110110: 3.20V 110111: 3.25V 111000: 3.30V 111001: 3.35V 111010: 3.40V 111011: 3.45V 111100: 3.50V 111101: 3.55V 111110: 3.60V 111111: 3.65V

0330 **ISINK0_CON0** **ISINK0 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ISINK0_RSV0									ISINK_CH0_MODE			
Type				RW									RW			
Reset				0	0	0	0	0					0	0		

Bit(s)	Mnemonic	Name	Description
12:8	**ISINK0_RSV0**	ISINK_DIM0_DUTY	**ISINK ON-duty of dimming 0 control** N: (N+1)/32 0: 1/32 1: 2/32

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Bit(s)	Mnemonic	Name	Description
			2: 3/32 31: 32/32
3:2		ISINK_CH0_MODE	**Selects ISINK Channel 0 enable mode** 00: PWM mode 01: Breath mode 10: Register mode 11: Register mode

0332 **ISINK0_CON1** **ISINK0 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ISINK_DIM0_FSEL**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		ISINK_DIM0_FSEL	**Selects ISINK0 dimming frequency** Backlight 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

0334 **ISINK0_CON2** **ISINK0 Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**ISINK_CH0_STEP**												**ISINK_CH0_STEP**		**ISINK_SFSTR0_EN**
Type		RW												RW		RW
Reset		0	0	0										0	0	0

Bit(s)	Mnemonic	Name	Description
14:12		ISINK_CH0_STEP	**Coarse 6 step current level for ISINK CH0** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA

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Bit(s)	Mnemonic	Name	Description
			110: 24mA 111: 24mA
2:1	**ISINK_CH0_STEP**	ISINK_SFSTR0_TC	**ISINK0 soft start timing step control** 0: 0.5us 1: 1us 2: 1.5us 3: 2us
0		ISINK_SFSTR0_EN	**ISNIK0 soft start control** 1: Enable soft start current step 0: Disable

0336 **ISINK0_CON3** **ISINK0 Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH0_TRF_SEL				ISINK_BREATH0_TRF_SEL								ISINK_BREATH0_TOFF_SEL			
Type	RW				RW								RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:12		ISINK_BREATH0_TRF_SEL	**Selects ISINK0 breath mode rising and falling time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	**ISINK_BREATH0_TRF_SEL**	ISINK_BREATH0_TON_SEL	**Selects ISINK0 breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s

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Bit(s)	Mnemonic	Name	Description
3:0		ISINK_BREATH0_TOFF_SEL	**Selects ISINK0 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0338 ISINK1_CON0 ISINK1 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ISINK1_RSV0									ISINK1_RSV1			
Type				RW									RW			
Reset				0	0	0	0	0					0	0		

Bit(s)	Mnemonic	Name	Description
12:8	**ISINK1_RSV0**	ISINK_DIM1_DUTY	**ISINK ON-duty of dimming 1 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32
3:2	**ISINK1_RSV1**	ISINK_CH1_MODE	**Selects ISINK Channel 1 enable mode** 00: PWM mode 01: Breath mode 10: Register mode 11: Register mode

033A ISINK1_CON1 ISINK1 Control Register 1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_DIM1_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		ISINK_DIM1_FSEL	**Selects ISINK1 dimming frequency** Backlight 2: 20kHz 61: 1kHz 311: 200Hz

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Bit(s)	Mnemonic	Name	Description
			12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

033C **ISINK1_CON2** **ISINK1 Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**ISINK_CH1_STEP**												**ISINK_CH1_STEP**		**ISINK_SFSTR1_EN**
Type		RW												RW		RW
Reset		0	0	0										0	0	0

Bit(s)	Mnemonic	Name	Description
14:12		ISINK_CH1_STEP	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
2:1	**ISINK_CH1_STEP**	ISINK_SFSTR1_TC	**ISNIK1 soft start timing step control** 0: 0.5us 1: 1us 2: 1.5us 3: 2us
0		ISINK_SFSTR1_EN	**ISNIK1 soft start control** 1: Enable soft start current step 0: Disable

033E **ISINK1_CON3** **ISINK1 Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ISINK_BREATH1_TRF_SEL**				**ISINK_BREATH1_TRF_SEL**								**ISINK_BREATH1_TOFF_SEL**			
Type	RW				RW								RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
15:12		ISINK_BREATH1_TRF_SEL	**Selects ISINK1 breath mode rising and falling time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	**ISINK_BREATH1_TRF_SEL**	ISINK_BREATH1_TON_SEL	**Selects ISINK1 breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0		ISINK_BREATH1_TOFF_SEL	**Selects ISINK1 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0340 **ISINK2_CON0** **ISINK2 Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**ISINK2_RSV0**									**ISINK2_RS**			

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0340 **ISINK2_CON0** **ISINK2 Control Register 0** **0000**

													V1			
Type				RW									RW			
Reset				0	0	0	0	0					0	0		

Bit(s)	Mnemonic	Name	Description
12:8	**ISINK2_RSV0**	ISINK_DIM2_DUTY	**ISINK ON-duty of dimming 2 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32
3:2	**ISINK2_RSV1**	ISINK_CH2_MODE	**Selects ISINK Channel 2 enable mode** 00: PWM mode 01: Breath mode 10: Register mode 11: Register mode

0342 **ISINK2_CON1** **ISINK2 Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ISINK_DIM2_FSEL**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		ISINK_DIM2_FSEL	**Selects ISINK2 dimming frequency** Backlight 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

0344 **ISINK2_CON2** **ISINK2 Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		**ISINK_CH2_STEP**												**ISINK_CH2_STEP**		**ISINK_SFSTR2_EN**
Type		RW												RW		RW

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0344	ISINK2_CON2	ISINK2 Control Register 2														0000
Reset		0	0	0										0	0	0

Bit(s)	Mnemonic	Name	Description
14:12		ISINK_CH2_STEP	**Coarse 6 step current level for ISINK CH2** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
2:1	**ISINK_CH2_STEP**	ISINK_SFSTR2_TC	**ISNIK2 soft start timing step control** 0: 0.5us 1: 1us 2: 1.5us 3: 2us
0		ISINK_SFSTR2_EN	**ISINK2 soft start control** 1: Enable sfter start current step 0: Disable

0346	ISINK2_CON3	ISINK2 Control Register 3														0000
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH2_TRF_SEL				ISINK_BREATH2_TRF_SEL								ISINK_BREATH2_TOFF_SEL			
Type	RW				RW								RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:12		ISINK_BREATH2_TRF_SEL	**Selects ISINK2 breath mode rising and falling time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	**ISINK_BREATH2_TRF_SEL**	ISINK_BREATH2_TON_SEL	**Selects ISINK2 breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s

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Bit(s)	Mnemonic	Name	Description
			5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0		ISINK_BREATH2_TOFF_SEL	**Selects ISINK2 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s 13: 5.351s 14: 5.720s 15: 6.151s

0348 ISINK3_CON0 ISINK3 Control Register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ISINK3_RSV0									ISINK3_RSV1			
Type				RW									RW			
Reset				0	0	0	0	0					0	0		

Bit(s)	Mnemonic	Name	Description
12:8	**ISINK3_RSV0**	ISINK_DIM3_DUTY	**ISINK ON-duty of dimming 3 control** N: (N+1)/32 0: 1/32 1: 2/32 2: 3/32 31: 32/32
3:2	**ISINK3_RSV1**	ISINK_CH3_MODE	**Selects ISINK Channel 3 enable mode** 00: PWM mode 01: Breath mode 10: Register mode 11: Register mode

034A ISINK3_CON1 ISINK3 Frequency Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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034A ISINK3_CON1 ISINK3 Frequency Register 0000

Name	ISINK_DIM3_FSEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		ISINK_DIM3_FSEL	**Selects ISINK3 dimming frequency** Backlight 2: 20kHz 61: 1kHz 311: 200Hz 12499: 5Hz 31249: 2Hz 62499: 1Hz Indicator 0: 1kHz 4: 200Hz 199: 5Hz 499: 2Hz 999: 1Hz 1999: 0.5Hz 4999: 0.2Hz 9999: 0.1Hz

034C ISINK3_CON2 ISINK3 Control Register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		ISINK_CH3_STEP												ISINK_CH3_STEP		ISINK_SFSTR3_EN
Type		RW												RW		RW
Reset		0	0	0										0	0	0

Bit(s)	Mnemonic	Name	Description
14:12		ISINK_CH3_STEP	**Coarse 6 step current level for ISINK CH3** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
2:1	**ISINK_CH3_STEP**	ISINK_SFSTR3_TC	**ISNIK3 soft start timing step control** 0: 0.5us 1: 1us 2: 1.5us 3: 2us
0		ISINK_SFSTR3_EN	**ISINK3 soft start control** 1: Enable sfter start current step 0: Disable

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034E	ISINK3_CON3	ISINK3 Control Register 3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ISINK_BREATH3_TRF_SEL				ISINK_BREATH3_TRF_SEL								ISINK_BREATH3_TOFF_SEL			
Type	RW				RW								RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:12		ISINK_BREATH3_TRF_SEL	**Selects ISINK3 breath mode rising and falling time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
11:8	**ISINK_BREATH3_TRF_SEL**	ISINK_BREATH3_TON_SEL	**Selects ISINK3 breath mode Ton time** 0: 0.123s 1: 0.338s 2: 0.523s 3: 0.707s 4: 0.926s 5: 1.107s 6: 1.291s 7: 1.507s 8: 1.691s 9: 1.876s 10: 2.091s 11: 2.276s 12: 2.460s 13: 2.676s 14: 2.860s 15: 3.075s
3:0		ISINK_BREATH3_TOFF_SEL	**Selects ISINK3 breath mode Toff time** 0: 0.246s 1: 0.677s 2: 1.046s 3: 1.417s 4: 1.845s 5: 2.214s 6: 2.583s 7: 3.014s 8: 3.383s 9: 3.752s 10: 4.183s 11: 4.552s 12: 4.921s

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Bit(s)	Mnemonic	Name	Description
			13: 5.351s 14: 5.720s 15: 6.151s

0350 **ISINK_ANA0** **ISINKS ACD Interface 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_ISINK0_double_EN**	**RG_ISINK1_double_EN**	**RG_ISINK2_double_EN**	**RG_ISINK3_double_EN**								
Type					RW	RW	RW	RW								
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11		RG_ISINK0_double_EN	**Coarse 6 step current level for ISINK CH0** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
10		RG_ISINK1_double_EN	**Coarse 6 step current level for ISINK CH1** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
9		RG_ISINK2_double_EN	**Coarse 6 step current level for ISINK CH2** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
8		RG_ISINK3_double_EN	**Coarse 6 step current level for ISINK CH3** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA

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0354	ISINK_PHASE_DLY	ISINK Phase Delay	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ISINK_PHASE_DLY_TC		ISINK_PHASE3_DLY_EN	ISINK_PHASE2_DLY_EN	ISINK_PHASE1_DLY_EN	ISINK_PHASE0_DLY_EN
Type											RW		RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:4		ISINK_PHASE_DLY_TC	**Selects ISINK channel backlight phase delay** 0: 0.5us 1: 1us 2: 1.5us 3: 2us
3		ISINK_PHASE3_DLY_EN	**ISINK3 phase delay control** 1: Enable phase delay 0: Disable
2		ISINK_PHASE2_DLY_EN	**ISINK2 phase delay control** 1: Enable phase delay 0: Disable
1		ISINK_PHASE1_DLY_EN	**ISINK1 phase delay control** 1: Enable phase delay 0: Disable
0		ISINK_PHASE0_DLY_EN	**ISINK0 phase delay control** 1: Enable phase delay 0: Disable

0356	ISINK_EN_CTRL	ISINK Enable Control	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ISINK_CHOP3_EN	ISINK_CHOP2_EN	ISINK_CHOP1_EN	ISINK_CHOP0_EN	ISINK_CH3_EN	ISINK_CH2_EN	ISINK_CH1_EN	ISINK_CH0_EN
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7		ISINK_CHOP3_EN	**Enables ISINK Channel 3 CHOP CLK** 0: Disable 1: Enable
6		ISINK_CHOP2_EN	**Enables ISINK Channel 2 CHOP CLK** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
5		ISINK_CHOP1_EN	**Enables ISINK Channel 1 CHOP CLK** 0: Disable 1: Enable
4		ISINK_CHOP0_EN	**Enables ISINK Channel 0 CHOP CLK** 0: Disable 1: Enable
3		ISINK_CH3_EN	**Turns on ISINK Channel 3** 0: Disable 1: Enable
2		ISINK_CH2_EN	**Turns on ISINK Channel 2** 0: Disable 1: Enable
1		ISINK_CH1_EN	**Turns on ISINK Channel 1** 0: Disable 1: Enable
0		ISINK_CH0_EN	**Turns on ISINK Channel 0** 0: Disable 1: Enable

0402 **ANALDO_CON1** **Analog LDO Control Register 1** **0400**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VTCXO_EN**															
Type	RO															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15	**QI_VTCXO_EN**	QI_VTCXO_EN	

0404 **ANALDO_CON2** **Analog LDO Control Register 2** **4000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VA_EN**								**QI_VA_MODE**							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VA_EN**	QI_VA_EN	
7	**QI_VA_MODE**	QI_VA_MODE	

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0408	ANALDO_CON4	Analog LDO Control Register 4	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCAMA_EN															
Type	RW															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15	RG_VCAMA_EN	RG_VCAMA_EN	**Enable** 1'b1: Enable 1'b0: Disable

040A	ANALDO_CON5	Analog LDO Control Register 5	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			QI_VTCXO_OC_STATUS		QI_VA_OC_STATUS			QI_VCAMA_OC_STATUS								
Type			RO		RO			RO								
Reset			0		0			0								

Bit(s)	Mnemonic	Name	Description
13	QI_VTCXO_OC_STATUS	QI_VTCXO_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
11	QI_VA_OC_STATUS	QI_VA_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
8	QI_VCAMA_OC_STATUS	QI_VCAMA_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current

0410	ANALDO_CON8	Analog LDO Control Register 8	0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_VA_VOSEL						

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0410 **ANALDO_CON8** **Analog LDO Control Register 8** **0004**

Type										RW						
Reset										0						

Bit(s)	Mnemonic	Name	Description
6	**RG_VA_VOSEL**	RG_VA_VOSEL	**Selects output voltage (removed)** 1'b0: 1.8V 1'b1: 2.5V

0412 **ANALDO_CON10** **Analog LDO Control Register 10** **0064**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_VCAMA_CAL**					**RG_VCAMA_VOSEL**					**RG_VCAMA_FBSEL**	
Type					RW					RW					RW	
Reset					0	0	0	0		1	1				0	0

Bit(s)	Mnemonic	Name	Description
11:8	**RG_VCAMA_CAL**	RG_VCAMA_CAL	**Calibrates voltage** 0000: 0mV 0001: -20mV 0010: -40mV 0011: -60mV 0100: -80mV 0101: -100mV 0110: -120mV 0111: -140mV 1000: 160mV 1001: 140mV 1010: 120mV 1011: 100mV 1100: 80mV 1101: 60mV 1110: 40mV 1111: 20mV
6:5	**RG_VCAMA_VOSEL**	RG_VCAMA_VOSEL	**Selects output voltage** 2'b00: 1.5V 2'b01: 1.8V 2b'10: 2.5V 2b'11: 2.8V
1:0	**RG_VCAMA_FBSEL**	RG_VCAMA_FBSEL	**Selects load regulation peformance** 2'b00: 18mV 2'b01: 8mV 2b'10: 12mV 2b'11: 30mV

0418 **ANALDO_CON17** **Analog LDO Control Register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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0418 ANALDO_CON17 Analog LDO Control Register 17 0000

Name	**QI_VCN33_EN**															
Type	RO															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15		QI_VCN33_EN	1'b1: Enable 1'b0: Eisable

041C ANALDO_CON19 Analog LDO Control Register 19 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VCN28_EN**			**RG_VCN28_EN**												
Type	RO			RW												
Reset	0			0												

Bit(s)	Mnemonic	Name	Description
15		QI_VCN28_EN	1'b1: enable 1'b0: disable
12		RG_VCN28_EN	**Enable** 1'b1: Enable 1'b0: Disable

041E ANALDO_CON20 Analog LDO Control Register 20 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VCN28_OC_STATUS**								**QI_VCN28_MODE**							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VCN28_OC_STATUS**	QI_VCN28_OC_STATUS	
7	**QI_VCN28_MODE**	QI_VCN28_MODE	**Enables low power mode** PMU_RSTB should not be used to gate D/A interface LS. 0: Normal mode

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Bit(s)	Mnemonic	Name	Description
			1: Low power mode

0420 **ANALDO_CON21** **Analog LDO Control Register 21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCN33_OC_STATUS			RG_VCN33_EN					QI_VCN33_MODE							
Type	RO			RW					RO							
Reset	0			0					0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VCN33_OC_STATUS**	QI_VCN33_OC_STATUS	
12		RG_VCN33_EN	**Enable** 1'b1: Enable 1'b0: Disable
7	**QI_VCN33_MODE**	QI_VCN33_MODE	**Enables low power mode** PMU_RSTB should not be used to gate D/A interface LS. 0: Normal mode 1: Low power mode

0500 **DIGLDO_CON0** **Digital LDO control register 0** **4000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VIO28_EN								QI_VIO28_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VIO28_EN**	QI_VIO28_EN	
7	**QI_VIO28_MODE**	QI_VIO28_MODE	

0502 **DIGLDO_CON2** **Digital LDO control register 2** **4000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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0502 **DIGLDO_CON2** **Digital LDO control register 2** **4000**

Name	**QI_VUSB_EN**								**QI_VUSB_MODE**							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VUSB_EN**	QI_VUSB_EN	
7	**QI_VUSB_MODE**	QI_VUSB_MODE	

0504 **DIGLDO_CON3** **Digital LDO control register 3** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VMC_EN**								**QI_VMC_MODE**							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VMC_EN**	QI_VMC_EN	
7	**QI_VMC_MODE**	QI_VMC_MODE	

0506 **DIGLDO_CON5** **Digital LDO control register 5** **4000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VMCH_EN**								**QI_VMCH_MODE**							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VMCH_EN**	QI_VMCH_EN	
7	**QI_VMCH_MODE**	QI_VMCH_MODE	

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0508	DIGLDO_CON6	Digital LDO control register 6	4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VEMC_3V3_EN								QI_VEMC_3V3_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VEMC_3V3_EN**	QI_VEMC_3V3_EN	
7	**QI_VEMC_3V3_MODE**	QI_VEMC_3V3_MODE	

050A	DIGLDO_CON7	Digital LDO control register 7	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									QI_VGP1_MODE						VGP1_LP_MODE_SET	VGP1_LP_SEL
Type									RO						RW	RW
Reset									0						0	0

Bit(s)	Mnemonic	Name	Description
7	**QI_VGP1_MODE**	QI_VGP1_MODE	
1	**VGP1_LP_MODE_SET**	VGP1_LP_MODE_SET	**Low power mode software setting** 0: Normal 1: Low power mode
0	**VGP1_LP_SEL**	VGP1_LP_SEL	**Selects low power mode** 1: SRCLKEN 0: SW control

050C	DIGLDO_CON8	Digital LDO control register 8	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VGP2_E								QI_VGP2_MO						VGP2_LP_MO	VGP2_LP_SEL

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	N								DE						DE_SET	
Type	RW								RO						RW	RW
Reset	0								0						0	0

Bit(s)	Mnemonic	Name	Description	
15	**RG_VGP2_EN**	RG_VGP2_EN	**Enable** 1'b1: 1'b0: Disable	Enable
7	**QI_VGP2_MODE**	QI_VGP2_MODE		
1	**VGP2_LP_MODE_SET**	VGP2_LP_MODE_SET	**Low power mode software setting** 0: 1: Low power mode	Normal
0	**VGP2_LP_SEL**	VGP2_LP_SEL	**Selects low power mode** 1: 0: SW control	SRCLKEN

050E DIGLDO_CON9 Digital LDO control register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VGP3_EN								QI_VGP3_MODE						VGP3_LP_MODE_SET	VGP3_LP_SEL
Type	RW								RO						RW	RW
Reset	0								0						0	0

Bit(s)	Mnemonic	Name	Description	
15	**RG_VGP3_EN**	RG_VGP3_EN	**Enable** 1'b1: 1'b0: Disable	Enable
7	**QI_VGP3_MODE**	QI_VGP3_MODE		
1	**VGP3_LP_MODE_SET**	VGP3_LP_MODE_SET	**Low power mode software setting** 0: 1: Low power mode	Normal
0	**VGP3_LP_SEL**	VGP3_LP_SEL	**Selects low power mode** 1: 0: SW control	SRCLKEN

0512 DIGLDO_CON11 Digital LDO Control Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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0512	DIGLDO_CON 11	Digital LDO Control Register 11	0000

Name	**QI_VCN_1V8_EN**								**QI_VCN_1V8_MODE**							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VCN_1V8_EN**	QI_VCN_1V8_EN	
7	**QI_VCN_1V8_MODE**	QI_VCN_1V8_MODE	

0516	DIGLDO_CON 13	Digital LDO Control Register 13	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_VSIM1_EN**								**QI_VSIM1_MODE**						**VSIM1_LP_MODE_SET**	**VSIM1_LP_SEL**
Type	RW								RO						RW	RW
Reset	0								0						0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_VSIM1_EN**	RG_VSIM1_EN	**Enable** 1'b1: Enable 1'b0: Disable
7	**QI_VSIM1_MODE**	QI_VSIM1_MODE	
1	**VSIM1_LP_MODE_SET**	VSIM1_LP_MODE_SET	**Low power mode software setting** 0: Normal 1: Low power mode
0	**VSIM1_LP_SEL**	VSIM1_LP_SEL	**Selects low power mode** 1: SRCLKEN 0: SW control

0518	DIGLDO_CON 14	Digital LDO Control Register 14	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**QI_VSIM2_MODE**					**VSIM2_THER_SHDN_E**	**VSIM2_LP_MODE_SET**	**VSIM2_LP_SEL**

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0518	DIGLDO_CON 14	Digital LDO Control Register 14	0000

														N		
Type									RO					RW	RW	RW
Reset									0					0	0	0

Bit(s)	Mnemonic	Name	Description
7	**QI_VSIM2_MODE**	QI_VSIM2_MODE	
2	**VSIM2_THER_SHDN_EN**	VSIM2_THER_SHDN_EN	**Enables VSIM2 thermal shut-down** 1'b1: Enable 1'b0: Disable
1	**VSIM2_LP_MODE_SET**	VSIM2_LP_MODE_SET	**Low power mode software setting** 0: Normal 1: Low power mode
0	**VSIM2_LP_SEL**	VSIM2_LP_SEL	**Selects low power mode** 1: SRCLKEN 0: SW control

051A	DIGLDO_CON 15	Digital LDO Control Register15	0100

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VRTC_EN**															
Type	RO															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15	**QI_VRTC_EN**	QI_VRTC_EN	

0520	DIGLDO_CON 18	Digital LDO Control Register 18	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VIO28_OC_STATUS**				**QI_VUSB_OC_STATUS**	**QI_VMC_OC_STATUS**				**QI_VMCH_OC_STATUS**			**QI_VEMC_3V3_OC_STATUS**			
Type	RO				RO	RO				RO			RO			
Reset	0				0	0				0			0			

Bit(s)	Mnemonic	Name	Description
15	**QI_VIO28_OC_STA**	QI_VIO28_OC_S	**Over-current status**

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Bit(s)	Mnemonic	Name	Description
	TUS	TATUS	1'b1: Over-current occurs. 1'b0: No over-current
11	**QI_VUSB_OC_STATUS**	QI_VUSB_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
10	**QI_VMC_OC_STATUS**	QI_VMC_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
6	**QI_VMCH_OC_STATUS**	QI_VMCH_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
3	**QI_VEMC_3V3_OC_STATUS**	QI_VEMC_3V3_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current

0522 **DIGLDO_CON19** **Digital LDO Control Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VGP1_OC_STATUS	QI_VGP2_OC_STATUS			QI_VGP3_OC_STATUS						QI_VIBR_OC_STATUS		QI_VSIM1_OC_STATUS	QI_VSIM2_OC_STATUS		
Type	RO	RO			RO						RO		RO	RO		
Reset	0	0			0						0		0	0		

Bit(s)	Mnemonic	Name	Description
15	**QI_VGP1_OC_STATUS**	QI_VGP1_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
14	**QI_VGP2_OC_STATUS**	QI_VGP2_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
11	**QI_VGP3_OC_STATUS**	QI_VGP3_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
5	**QI_VIBR_OC_STATUS**	QI_VIBR_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
3	**QI_VSIM1_OC_STATUS**	QI_VSIM1_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
2	**QI_VSIM2_OC_STATUS**	QI_VSIM2_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current

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0524 **DIGLDO_CON 20** **Digital LDO Control Register 20** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RE_DIGLDORSV2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Mnemonic	Name	Description
15:1	**RE_DIGLDORSV2**	RE_DIGLDORSV2	

0530 **DIGLDO_CON 28** **Digital LDO Control Register 28** **00A1**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VGP1_CAL				RG_VGP1_VOSEL							
Type					RW				RW							
Reset					0	0	0	0	1	0	1					

Bit(s)	Mnemonic	Name	Description
11:8	**RG_VGP1_CAL**	RG_VGP1_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV (unused for 1.3V output, -0mV) 4'b0101: -100mV (unused for 1.3V output, -20mV) 4'b0110: -120mV (unused for 1.3V output, -40mV) 4'b0111: -140mV (unused for 1.3V output, -60mV) 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
7:5	**RG_VGP1_VOSEL**	RG_VGP1_VOSEL	**Output selection signal** (3'b101: 2.8V) 3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.0V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 3.3V

0532 **DIGLDO_CON 29** **Digital LDO Control Register 29** **0081**

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0532 DIGLDO_CON29 Digital LDO Control Register 29 0081

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VGP2_CAL				RG_VGP2_VOSEL							
Type					RW				RW							
Reset					0	0	0	0	1	0	0					

Bit(s)	Mnemonic	Name	Description
11:8	RG_VGP2_CAL	RG_VGP2_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV (unused for 1.3V output, -0mV) 4'b0101: -100mV (unused for 1.3V output, -20mV) 4'b0110: -120mV (unused for 1.3V output, -40mV) 4'b0111: -140mV (unused for 1.3V output, -60mV) 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
7:5	RG_VGP2_VOSEL	RG_VGP2_VOSEL	**Output selection signal** (3'b100: 2.8V) 3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.5V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 2.0V

0534 DIGLDO_CON30 Digital LDO Control Register 30 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VGP3_CAL					RG_VGP3_VOSEL						
Type					RW					RW						
Reset					0	0	0	0		0	0					

Bit(s)	Mnemonic	Name	Description
11:8	RG_VGP3_CAL	RG_VGP3_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV (unused for 1.3V output, -0mV) 4'b0101: -100mV (unused for 1.3V output, -20mV) 4'b0110: -120mV (unused for 1.3V output, -40mV)

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Bit(s)	Mnemonic	Name	Description
			4'b0111: -140mV (unused for 1.3V output, -60mV) 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
6:5	**RG_VGP3_VOSEL**	RG_VGP3_VOSEL	**Output selection signal** (2'b00: 2.8V) 2'b00: 1.2V 2'b01: 1.3V 2'b10: 1.5V 2'b11: 1.8V

0536 DIGLDO_CON31 Digital LDO Control Register 31 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCAM_AF_EN								QI_VCAM_AF_MODE						VCAM_AF_LP_MODE_SET	VCAM_AF_LP_SEL
Type	RW								RO						RW	RW
Reset	0								0						0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_VCAM_AF_EN**	RG_VCAM_AF_EN	**Enable** 1'b1: Enable 1'b0: Disable
7	**QI_VCAM_AF_MODE**	QI_VCAM_AF_MODE	
1	**VCAM_AF_LP_MODE_SET**	VCAM_AF_LP_MODE_SET	**Low power mode software setting** 0: Normal 1: Low power mode
0	**VCAM_AF_LP_SEL**	VCAM_AF_LP_SEL	**Selects low power mode** 1: SRCLKEN 0: SW control

0538 DIGLDO_CON32 Digital LDO Control Register 32 0081

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_VCAM_AF_CAL							RG_VCAM_AF_VOSEL				VCAM_AF_O			

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0538 **DIGLDO_CON 32** **Digital LDO Control Register 32** **0081**

													N_CTRL			
Type		RW							RW				RW			
Reset		0	0	0	0				1	0	0		0			

Bit(s)	Mnemonic	Name	Description
14:11	**RG_VCAM_AF_CAL**	RG_VCAM_AF_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV (unused for 1.3V output, -0mV) 4'b0101: -100mV (unused for 1.3V output, -20mV) 4'b0110: -120mV (unused for 1.3V output, -40mV) 4'b0111: -140mV (unused for 1.3V output, -60mV) 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
7:5	**RG_VCAM_AF_VOSEL**	RG_VCAM_AF_VOSEL	**Output selection signal** (3'b101: 2.8V) 3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.0V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 3.3V
3		VCAM_AF_ON_CTRL	1'b0: SW control 1'b1: HW control

053C **DIGLDO_CON 34** **Digital LDO Control Register 34** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VSIM1_CAL						RG_VSIM1_VOSEL					
Type					RW						RW					
Reset					0	0	0	0			0					

Bit(s)	Mnemonic	Name	Description
11:8	**RG_VSIM1_CAL**	RG_VSIM1_CAL	**Calibrates voltage** 4'b0000: 0mV

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Bit(s)	Mnemonic	Name	Description
			4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV (unused for 1.3V output, -0mV) 4'b0101: -100mV (unused for 1.3V output, -20mV) 4'b0110: -120mV (unused for 1.3V output, -40mV) 4'b0111: -140mV (unused for 1.3V output, -60mV) 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
5	**RG_VSIM1_VOSEL**	RG_VSIM1_VOSEL	**Output selection signal** 1'b0: 1.8V 1'b1: 3.0V

053E **DIGLDO_CON35** **Digital LDO Control Register 35** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_VSIM2_CAL**						**RG_VSIM2_VOSEL**					
Type					RW						RW					
Reset					0	0	0	0			0					

Bit(s)	Mnemonic	Name	Description
11:8	**RG_VSIM2_CAL**	RG_VSIM2_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV (unused for 1.3V output, -0mV) 4'b0101: -100mV (unused for 1.3V output, -20mV) 4'b0110: -120mV (unused for 1.3V output, -40mV) 4'b0111: -140mV (unused for 1.3V output, -60mV) 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
5	**RG_VSIM2_VOSEL**	RG_VSIM2_VOSEL	**Output selection signal** 1'b0: 1.8V 1'b1: 3.0V

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0542	DIGLDO_CON39	Digital LDO Control Register 39	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VIBR_EN								QI_VIBR_MODE						VIBR_LP_MODE_SET	VIBR_LP_SEL
Type	RW								RO						RW	RW
Reset	0								0						0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_VIBR_EN**	RG_VIBR_EN	**Enable** 1'b1: Enable 1'b0: Disable
7	**QI_VIBR_MODE**	QI_VIBR_MODE	
1	**VIBR_LP_MODE_SET**	VIBR_LP_MODE_SET	**Low power mode software setting** 0: Normal 1: Low power mode
0	**VIBR_LP_SEL**	VIBR_LP_SEL	**Selects low power mode** 1: SRCLKEN 0: SW control

0544	DIGLDO_CON40	Digital LDO Control Register 40	0101

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_VIBR_CAL						RG_VIBR_VOSEL							
Type			RW						RW							
Reset			0	0	0	0			0	0	0					

Bit(s)	Mnemonic	Name	Description
13:10	**RG_VIBR_CAL**	RG_VIBR_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV (unused for 1.3V output, -0mV) 4'b0101: -100mV (unused for 1.3V output, -20mV) 4'b0110: -120mV (unused for 1.3V output, -40mV) 4'b0111: -140mV (unused for 1.3V output, -60mV) 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
7:5	**RG_VIBR_VOSEL**	RG_VIBR_VOSEL	**Output selection signal** (3'b100: 2.8V)

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Bit(s)	Mnemonic	Name	Description
			3'b000: 1.2V 3'b001: 1.3V 3'b010: 1.5V 3'b011: 1.8V 3'b100: 2.0V 3'b101: 2.8V 3'b110: 3.0V 3'b111: 3.3V

0548 **DIGLDO_CON42** **Digital LDO Control Register 42** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCAM_AF_OC_STATUS		QI_VM_OC_STATUS		QI_VRF18_OC_STATUS		QI_VIO18_OC_STATUS		QI_VCN_1V8_OC_STATUS		QI_VCAMD_OC_STATUS		QI_VCAM_IO_OC_STATUS			
Type	RO		RO		RO		RO		RO		RO		RO			
Reset	0		0		0		0		0		0		0			

Bit(s)	Mnemonic	Name	Description
15	**QI_VCAM_AF_OC_STATUS**	QI_VCAM_AF_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
13	**QI_VM_OC_STATUS**	QI_VM_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
11	**QI_VRF18_OC_STATUS**	QI_VRF18_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
9	**QI_VIO18_OC_STATUS**	QI_VIO18_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
7	**QI_VCN_1V8_OC_STATUS**	QI_VCN_1V8_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
5	**QI_VCAMD_OC_STATUS**	QI_VCAMD_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current
3	**QI_VCAM_IO_OC_STATUS**	QI_VCAM_IO_OC_STATUS	**Over-current status** 1'b1: Over-current occurs. 1'b0: No over-current

054C **DIGLDO_CON44** **Digital LDO Control Register 44** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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054C DIGLDO_CON44 Digital LDO Control Register 44 0000

Name	**VGP1_ON_CTRL**	**VGP2_ON_CTRL**	**VGP3_ON_CTRL**				**VSIM1_ON_CTRL**	**VSIM2_ON_CTRL**	**VIBR_ON_CTRL**							
Type	RW	RW	RW				RW	RW	RW							
Reset	0	0	0				0	0	0							

Bit(s)	Mnemonic	Name	Description
15		VGP1_ON_CTRL	0: SW controlled by RG_VGP1_EN 1: HW control
14		VGP2_ON_CTRL	0: SW controlled by RG_VGP2_EN 1: HW
13		VGP3_ON_CTRL	0: SW controlled by RG_VGP3_EN 1: HW
9		VSIM1_ON_CTRL	0: SW controlled by RG_VSIM1_EN 1: HW
8		VSIM2_ON_CTRL	0: SW controlled by RG_VSIM2_EN 1: HW
7		VIBR_ON_CTRL	0: SW controlled by RG_VIBR_EN 1: HW

054E DIGLDO_CON45 Digital LDO Control Register 45 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**QI_VRF18_MODE**							
Type									RO							
Reset									0							

Bit(s)	Mnemonic	Name	Description
7	**QI_VRF18_MODE**	QI_VRF18_MODE	

0552 DIGLDO_CON47 Digital LDO Control Register 47 4000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**QI_VM_EN**								**QI_VM_MODE**							
Type	RO								RO							
Reset	0								0							

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Bit(s)	Mnemonic	Name	Description
15	**QI_VM_EN**	QI_VM_EN	
7	**QI_VM_MODE**	QI_VM_MODE	

0556 **DIGLDO_CON49** **Digital LDO Control Register 49** **4000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VIO18_EN								QI_VIO18_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**QI_VIO18_EN**	QI_VIO18_EN	
7	**QI_VIO18_MODE**	QI_VIO18_MODE	

055A **DIGLDO_CON51** **Digital LDO Control Register 51** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCAMD_EN	RG_VCAMD_EN							QI_VCAMD_MODE						VCAMD_LP_MODE_SET	VCAMD_LP_SEL
Type	RO	RW							RO						RW	RW
Reset	0	0							0						0	0

Bit(s)	Mnemonic	Name	Description
15	**QI_VCAMD_EN**	QI_VCAMD_EN	
14	**RG_VCAMD_EN**	RG_VCAMD_EN	**Enable** 1: Enable 0: Disable
7	**QI_VCAMD_MODE**	QI_VCAMD_MODE	
1	**VCAMD_LP_MODE_SET**	VCAMD_LP_MODE_SET	**Low power mode software setting** 0: Normal 1: Low power mode
0	**VCAMD_LP_SEL**	VCAMD_LP_SEL	**Selects low power mode** 1: SRCLKEN 0: SW control

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055C **DIGLDO_CON52** **Digital LDO Control Register 52** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMD_CAL					RG_VCAMD_VOSEL					VCAMD_ON_CTRL	
Type					RW					RW					RW	
Reset					0	0	0	0		0	0				0	

Bit(s)	Mnemonic	Name	Description
11:8	**RG_VCAMD_CAL**	RG_VCAMD_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
6:5		RG_VCAMD_VOSEL	**Output selection signal** 2'b00: 1.2V 2'b01: 1.35V 2'b10: 1.5V 2'b11: 1.8V
1		VCAMD_ON_CTRL	0: SW control 1: HW

055E **DIGLDO_CON53** **Digital LDO Control Register 53** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_VCAMIO_EN	RG_VCAMIO_EN							QI_VCAMIO_MODE						VCAMIO_LP_MODE_SET	VCAMIO_LP_SEL
Type	RO	RW							RO						RW	RW
Reset	0	0							0						0	0

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Bit(s)	Mnemonic	Name	Description
15	**QI_VCAM_IO_EN**	QI_VCAM_IO_EN	
14	**RG_VCAM_IO_EN**	RG_VCAM_IO_EN	**Enable** 1: Enable 0: Disable
7	**QI_VCAM_IO_MODE**	QI_VCAM_IO_MODE	
1	**VCAM_IO_LP_MODE_SET**	VCAM_IO_LP_MODE_SET	**Low power mode software setting** 0: Normal 1: Low power mode
0	**VCAM_IO_LP_SEL**	VCAM_IO_LP_SEL	**Selects low power mode** 1: SRCLKEN 0: SW control

0560 **DIGLDO_CON54** **Digital LDO Control Register 54** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RG_VCAM_IO_CAL**										**VCAM_IO_ON_CTRL**	
Type					RW										RW	
Reset					0	0	0	0							0	

Bit(s)	Mnemonic	Name	Description
11:8	**RG_VCAM_IO_CAL**	RG_VCAM_IO_CAL	**Calibrates voltage** 4'b0000: 0mV 4'b0001: -20mV 4'b0010: -40mV 4'b0011: -60mV 4'b0100: -80mV 4'b0101: -100mV 4'b0110: -120mV 4'b0111: -140mV 4'b1000: +160mV 4'b1001: +140mV 4'b1010: +120mV 4'b1011: +100mV 4'b1100: +80mV 4'b1101: +60mV 4'b1110: +40mV 4'b1111: +20mV
1		VCAM_IO_ON_CTRL	0: SW control 1: HW

0600 **EFUSE_CON0** **EFUSE Control Register 0** **0000**

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0600 **EFUSE_CON0** **EFUSE Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_EFUSE_ADDR				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0	RG_EFUSE_ADDR	RG_EFUSE_ADDR	EFUSE address

0602 **EFUSE_CON1** **EFUSE Control Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_EFUSE_PROG					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0	RG_EFUSE_PROG	RG_EFUSE_PROG	Enables EFUSE program

0604 **EFUSE_CON2** **EFUSE Control Registerr 2** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_EFUSE_EN
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0	RG_EFUSE_EN	RG_EFUSE_EN	**EFUSE macro enabling bit** 0: Disable 1: Enable

0606 **EFUSE_CON3** **EFUSE Control Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_PKEY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_PKEY	RG_EFUSE_PKEY	EFUSE program protect key

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0608 EFUSE_CON4 EFUSE Control Register 4 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_EFUSE_RD_TRIG
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	RG_EFUSE_RD_TRIG	RG_EFUSE_RD_TRIG	EFUSE read trigger bit

060A EFUSE_CON5 EFUSE Control Register 5 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_RD_RDY_BYPASS		RG_SKIP_EFUSE_OUT		RG_EFUSE_PROG_SRC
Type												RW		RW		RW
Reset												0		0		0

Bit(s)	Mnemonic	Name	Description
4	RG_RD_RDY_BYPASS	RG_RD_RDY_BYPASS	0: Read delay bypass off 1: Read delay bypass on
2	RG_SKIP_EFUSE_OUT	RG_SKIP_EFUSE_OUT	0: Use EFUSE out 1: Skip EFUSE out
0	RG_EFUSE_PROG_SRC	RG_EFUSE_PROG_SRC	0: From pad 1: From register

060C EFUSE_CON6 EFUSE Control Register 6 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_EFUSE_BUSY		RG_EFUSE_RD_ACK
Type														RO		RO
Reset														0		0

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Bit(s)	Mnemonic	Name	Description
2	**RG_EFUSE_BUSY**	RG_EFUSE_BUSY	0: EFUSE controller is idle. 1: EFUSE controller is busy.
0	**RG_EFUSE_RD_ACK**	RG_EFUSE_RD_ACK	1: Read EFUSE done

060E **EFUSE_VAL_0_15** **EFUSE val 0 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_EFUSE_VAL_0_15**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_VAL_0_15**	RG_EFUSE_VAL_0_15	

0610 **EFUSE_VAL_16_31** **EFUSE val 16 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_EFUSE_VAL_16_31**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_VAL_16_31**	RG_EFUSE_VAL_16_31	

0612 **EFUSE_VAL_32_47** **EFUSE val 32 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_EFUSE_VAL_32_47**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_VAL_32_47**	RG_EFUSE_VAL_32_47	

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0614 **EFUSE_VAL_48_63** **EFUSE val 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_VAL_48_63															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_VAL_48_63	RG_EFUSE_VAL_48_63	

0616 **EFUSE_VAL_64_79** **EFUSE val 64 79** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_VAL_64_79															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_VAL_64_79	RG_EFUSE_VAL_64_79	

0618 **EFUSE_VAL_80_95** **EFUSE val 80 95** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_VAL_80_95															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_VAL_80_95	RG_EFUSE_VAL_80_95	

061A **EFUSE_VAL_96_111** **EFUSE val 96 111** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_VAL_96_111															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_VAL_96	RG_EFUSE_VAL	

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Bit(s)	Mnemonic	Name	Description
	_111	_96_111	

061C **EFUSE_VAL_112_127** **EFUSE val 112 127** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_EFUSE_VAL_112_127**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_VAL_112_127**	RG_EFUSE_VAL_112_127	

061E **EFUSE_VAL_128_143** **EFUSE val 128 143** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_EFUSE_VAL_128_143**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_VAL_128_143**	RG_EFUSE_VAL_128_143	

0620 **EFUSE_VAL_144_159** **EFUSE val 144 159** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_EFUSE_VAL_144_159**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_VAL_144_159**	RG_EFUSE_VAL_144_159	

0622 **EFUSE_VAL_160_175** **EFUSE val 160 175** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_EFUSE_VAL_160_175**															
Type	RW															

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0622	EFUSE_VAL_160_175	EFUSE val 160 175	0000

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_VAL_160_175	RG_EFUSE_VAL_160_175	

0624	EFUSE_VAL_176_191	EFUSE val 176 191	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_VAL_176_191															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_VAL_176_191	RG_EFUSE_VAL_176_191	

0626	EFUSE_DOUT_0_15	EFUSE dout 0 15	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_0_15															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_0_15	RG_EFUSE_DOUT_0_15	

0628	EFUSE_DOUT_16_31	EFUSE dout 16 31	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_16_31															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_16_31	RG_EFUSE_DOUT_16_31	

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062A **EFUSE_DOUT_32_47** **EFUSE dout 32 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_32_47															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_32_47	RG_EFUSE_DOUT_32_47	

062C **EFUSE_DOUT_48_63** **EFUSE dout 48 63** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_48_63															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_48_63	RG_EFUSE_DOUT_48_63	

062E **EFUSE_DOUT_64_79** **EFUSE dout 64 79** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_64_79															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_64_79	RG_EFUSE_DOUT_64_79	

0630 **EFUSE_DOUT_80_95** **EFUSE dout 80 95** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_80_95															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_DOUT_80_95**	RG_EFUSE_DOUT_80_95	

0632 EFUSE_DOUT_96_111 EFUSE dout 111 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_96_111															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_DOUT_96_111**	RG_EFUSE_DOUT_96_111	

0634 EFUSE_DOUT_112_127 EFUSE dout 112 127 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_112_127															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_DOUT_112_127**	RG_EFUSE_DOUT_112_127	

0636 EFUSE_DOUT_128_143 EFUSE dout 128 143 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_128_143															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_EFUSE_DOUT_128_143**	RG_EFUSE_DOUT_128_143	

0638 EFUSE_DOUT_144_159 EFUSE dout 144 159 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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0638	EFUSE_DOUT_144_159	EFUSE dout 144 159	0000

Name	RG_EFUSE_DOUT_144_159															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_144_159	RG_EFUSE_DOUT_144_159	

063A	EFUSE_DOUT_160_175	EFUSE dout 160 175	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_160_175															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_160_175	RG_EFUSE_DOUT_160_175	

063C	EFUSE_DOUT_176_191	EFUSE dout 176 191	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_EFUSE_DOUT_176_191															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_EFUSE_DOUT_176_191	RG_EFUSE_DOUT_176_191	

063E	EFUSE_CON7	EFUSE Control Register 7	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PA	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	RG_OTP_PA	RG_OTP_PA	

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0640 EFUSE_CON8 EFUSE Control Register 8 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_OTP_PDIN							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**RG_OTP_PDIN**	RG_OTP_PDIN	

0642 EFUSE_CON9 EFUSE Control Register 9 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															RG_OTP_PTM	
Type															RW	
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1:0	**RG_OTP_PTM**	RG_OTP_PTM	

0700 AUDTOP_CON0 AUDIO_TOP Config Register 0 6010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_AUDULL_CHS_EN	RG_AUDULL_VCMSEL	RG_AUDULL_VCM14_EN	RG_AUDULL_VREF24_EN	RG_AUDULL_VADC_DVREF_CAL	RG_AUDULL_VADC_DENB	RG_AUDULL_VPWDB_ADC	RG_AUDULL_VPWDB_PGA	RG_AUDULL_VUPG			RG_AUDULL_VCFG			
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW			RW			
Reset		1	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
14	**RG_AUDULL_CHS_EN**	RG_AUDULL_CHS_EN	**Enables UplinkL chopper** 0: Disable CHS 1: Enable CHS
13	**RG_AUDULL_VCMSEL**	RG_AUDULL_VCMSEL	**UplinkL Select 1.4V common mode voltage** 0: VCM = 1.41V 1: VCM = 1.36V
12	**RG_AUDULL_VCM14_EN**	RG_AUDULL_VCM14_EN	**UplinkL Enable 1.4V common mode voltage** 0: Disable 1: Enable
11	**RG_AUDU**	RG_AUDULL_VR	**UplinkL Enable 2.4V differential reference**

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Bit(s)	Mnemonic	Name	Description
	LL_VREF24_EN	EF24_EN	0: Disable 1: Enable
10	RG_AUDULL_VADC_DVREF_CAL	RG_AUDULL_VADC_DVREF_CAL	**Calibrates UplinkL ADC Dither reference voltage** 1: +/- 0.373V 0: +/- 0.56V
9	RG_AUDULL_VADC_DENB	RG_AUDULL_VADC_DENB	**Enables UplinkL ADC dither** 1: Disable dither 0: Enable dither
8	RG_AUDULL_VPWDB_ADC	RG_AUDULL_VPWDB_ADC	**UplinkL power down ADC** 1: Active 0: Power down
7	RG_AUDULL_VPWDB_PGA	RG_AUDULL_VPWDB_PGA	**UplinkL power down PGA** 1: Active 0: Power down
6:4	RG_AUDULL_VUPG	RG_AUDULL_VUPG	**Adjusts UplinkL PGA gain (6dB/step)** 000: -6dB 001: 0dB 010: +6dB 011: +12dB 100: +18dB 101: +24dB 110: N/A 111: N/A
3:0	RG_AUDULL_VCFG	RG_AUDULL_VCFG	**UplinkL RG_VCFG[0]: Selects PGA input** 1: MIC1 0: MIC0 RG_VCFG[3:1]: N/A

0702 **AUDTOP_CON1** **AUDIO_TOP Config Register 1** **0100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_AUDULR_VUPG			RG_AUDULR_VCFG					RG_AUDULL_VCALI		
Type						RW			RW					RW		
Reset						0	0	1	0	0	0	0		0	0	0

Bit(s)	Mnemonic	Name	Description
10:8	RG_AUDULR_VUPG	RG_AUDULR_VUPG	**Adjusts UplinkR PGA gain (6dB/step)** 000: -6dB 001: 0dB 010: +6dB 011: +12dB 100: +18dB 101: +24dB 110: N/A 111: N/A
7:4	RG_AUDULR_VCFG	RG_AUDULR_VCFG	**UplinkR RG_VCFG[0]: Selects PGA input** 1: MIC1 0: MIC0 RG_VCFG[3:1]: N/A

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Bit(s)	Mnemonic	Name	Description
2:0	**RG_AUDULL_VCALI**	RG_AUDULL_VCALI	**UplinkL Voice Uplink bias current calibration bits** 000: 1X 001: 0.8X 010: 0.67X 011: 0.57X 100: 1.25X 101: 1.5X 110: 1.75X 111: 2X

0704 **AUDTOP_CON2** **AUDIO_TOP Config Register 2** **00C0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RG_AUDULR_CHS_EN**	**RG_AUDULR_VCMSEL**	**RG_AUDULR_VCM14_EN**	**RG_AUDULR_VREF24_EN**	**RG_AUDULR_VADC_DVREF_CAL**	**RG_AUDULR_VADC_DENB**	**RG_AUDULR_VPWDB_ADC**	**RG_AUDULR_VPWDB_PGA**
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									1	1	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7	**RG_AUDULR_CHS_EN**	RG_AUDULR_CHS_EN	**Enables UplinkR choppere** 0: Disable CHS 1: Enable CHS
6	**RG_AUDULR_VCMSEL**	RG_AUDULR_VCMSEL	**UplinkR Select 1.4V common mode voltage** 0: VCM = 1.41V 1: VCM = 1.36V
5	**RG_AUDULR_VCM14_EN**	RG_AUDULR_VCM14_EN	**UplinkR Enable 1.4V common mode voltage** 0: Disable 1: Enable
4	**RG_AUDULR_VREF24_EN**	RG_AUDULR_VREF24_EN	**UplinkR Enable 2.4V differential reference** 0: Disable 1: Enable
3	**RG_AUDULR_VADC_DVREF_CAL**	RG_AUDULR_VADC_DVREF_CAL	**Calibrates UplinkR ADC Dither reference voltage** 1: +/- 0.373V 0: +/- 0.56V
2	**RG_AUDULR_VADC_DENB**	RG_AUDULR_VADC_DENB	**Enables UplinkR ADC dither** 1: Disable dither 0: Enable dither
1	**RG_AUDULR_VPWDB_ADC**	RG_AUDULR_VPWDB_ADC	**UplinkR power down ADC** 1: Active 0: Power down
0	**RG_AUDULR_VPWD**	RG_AUDULR_VPWDB_PGA	**UplinkR power down PGA** 1: Active

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Bit(s)	Mnemonic	Name	Description
	B_PGA		0: Power down

0706	AUDTOP_CON3	AUDIO_TOP Config Register 3	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_AUDULR_VCALI		
Type														RW		
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2:0	RG_AUDULR_VCALI	RG_AUDULR_VCALI	**UplinkR Voice Uplink bias current calibration bits** 000: 1X 001: 0.8X 010: 0.67X 011: 0.57X 100: 1.25X 101: 1.5X 110: 1.75X 111: 2X

0708	AUDTOP_CON4	AUDIO_TOP Config Register 4	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_AOUTR_PWDB	RG_AOUTL_PWDB	RG_ABIAS_PWDB	RG_ADACR_PWDB	RG_ADACL_PWDB	RG_AMUTEL	RG_AMUTER
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6	RG_AOUTR_PWDB	RG_AOUTR_PWDB	Powers down right channel output buffer
5	RG_AOUTL_PWDB	RG_AOUTL_PWDB	Powers down left channel output buffer
4	RG_ABIAS_PWDB	RG_ABIAS_PWDB	Powers down bias circuit
3	RG_ADACR_PWDB	RG_ADACR_PWDB	Powers down right channel
2	RG_ADACL_PWDB	RG_ADACL_PWDB	Powers down left channel
1	RG_AMUTEL	RG_AMUTEL	Mutes left channel
0	RG_AMUTER	RG_AMUTER	Mutes right channel

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070A **AUDTOP_CON5** **AUDIO_TOP Config Register 5** **1100**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RG_APGL				RG_APGR										
Type		RW				RW										
Reset		0	0	1		0	0	1								

Bit(s)	Mnemonic	Name	Description
14:12	**RG_APGL**	RG_APGL	Controls audio right channel amplifier gain
10:8	**RG_APGR**	RG_APGR	Controls audio left channel amplifier gain

070C **AUDTOP_CON6** **AUDIO_TOP Config Register 6** **1C32**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDDL_VREF24_EN	RG_AVCMGEN_EN		RG_DEPOP_CURSEL			RG_DEPOP_VCM_EN	RG_ADEPOPX		RG_ADEPOPX_EN			RG_AHFMODE			
Type	RW	RW		RW			RW	RW		RW			RW			
Reset	0	0		1	1		0	0	0	0			0			

Bit(s)	Mnemonic	Name	Description
15	**RG_AUDDL_VREF24_EN**	RG_AUDDL_VREF24_EN	**Downlink Enable 2.4V differential reference** 0: Disable 1: Enable
14	**RG_AVCMGEN_EN**	RG_AVCMGEN_EN	**Enables audio 1.4V halfV buffer** 0: Disable 1: Enable
12:11	**RG_DEPOP_CURSEL**	RG_DEPOP_CURSEL	**Selects depop charge/discharge current** 00: 10uA for 10uF cap. charge/discharge 01: 20uA for 22uF cap. charge/discharge 10: 30uA for 33uF cap. charge/discharge 11: 40uA for 47uF cap. charge/discharge
9	**RG_DEPOP_VCM_EN**	RG_DEPOP_VCM_EN	**Enables depop 1.4V common mode voltage** 0: Disable 1: Enable
8:7	**RG_ADEPOPX**	RG_ADEPOPX	**Powers on depop removal circuit resistor calibration** 00: 500 Ohm 01: 250 Ohm 10: 125 Ohm 11: 62.5 Ohm
6	**RG_ADEPOPX_EN**	RG_ADEPOPX_EN	**Powers on depop removal circuit** 0: Disable 1: Enable

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Bit(s)	Mnemonic	Name	Description
3	**RG_AHFMODE**	RG_AHFMODE	**Enables handsfree mode** 0: Normal audio mode 1: Support handsfree mode

070E **AUDTOP_CON7** **AUDIO_TOP Config Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RG_HSOUTSTBENH	RG_V2SPK	RG_VDEPOP	RG_VBUF_BIAS		RG_VBUF_PWDB	RG_VDPG							
Type			RW	RW	RW	RW		RW	RW							
Reset			0	0	0	0	0	0	0	0	0	0				

Bit(s)	Mnemonic	Name	Description
13	**RG_HSOUTSTBENH**	RG_HSOUTSTBENH	**Enables voice buffer output stability enhancement** 0: Enable 1: Disable
12	**RG_V2SPK**	RG_V2SPK	**Configures voice buffer output** 0: Connect to receiver 1: Connect to internal loud speaker
11	**RG_VDEPOP**	RG_VDEPOP	**Enables anti-pop for buffer output** 0: Disable 1: Enable
10:9	**RG_VBUF_BIAS**	RG_VBUF_BIAS	**Controls voice BUF bias** 00: 3X 01: 4X 10: 1X 11: 2X
8	**RG_VBUF_PWDB**	RG_VBUF_PWDB	**Powers down voice BUF** 0: Power down 1: Active
7:4	**RG_VDPG**	RG_VDPG	**Voice BUF Gain setting bit** 4'd0 ~ 4'd2: Prohibited 4'd3 ~ 4'd15: -22 + 2*N

0710 **AUDTOP_CON8** **AUDIO_TOP Config Register 8** **0200**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_AUDSPAREVMIC				RG_AUDMICBIASVREF		RG_AUDDIGMICBIAS		RG_AUDDIGMICNDUTY		RG_AUDDIGMICPDUTY		RG_AUDPWDBMICBIAS	RG_AUDDIGMICEN		
Type	RW				RW		RW		RW		RW		RW	RW		

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Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0		

Bit(s)	Mnemonic	Name	Description
15:12	**RG_AUDSPAREVMIC**	RG_AUDSPAREVMIC	**Spare control bits for AVDD25MIC voltage domain**
11:10	**RG_AUDMICBIASVREF**	RG_AUDMICBIASVREF	**Selects MIC bias output voltage** 0: 1.9V 01: 2.0V 10: 2.1V 11: 2.2V
9:8	**RG_AUDDIGMICBIAS**	RG_AUDDIGMICBIAS	**Controld digital microphone slew rate** 11>10>01>00
7:6	**RG_AUDDIGMICNDUTY**	RG_AUDDIGMICNDUTY	**Controld digital microphone negative duty**
5:4	**RG_AUDDIGMICPDUTY**	RG_AUDDIGMICPDUTY	**Controls digital microphone positive duty**
3	**RG_AUDPWDBMICBIAS**	RG_AUDPWDBMICBIAS	**Powers down MIC bias** 0: Power down 1: Power on
2	**RG_AUDDIGMICEN**	RG_AUDDIGMICEN	**Enables digital microphone** 0: Disable 1: Enable

0712 **AUDTOP_CON9** **AUDIO_TOP Config Register 9** **0018**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VBIRX_ZCD_STATUS				RG_VBIRX_ZCD_HYS_ENB	RG_VBIRX_ZCD_CALI		RG_VBIRX_ZCD_EN
Type									RO				RW	RW		RW
Reset									0	0	0	1	1	0	0	0

Bit(s)	Mnemonic	Name	Description
7:4	**RG_VBIRX_ZCD_STATUS**	RG_VBIRX_ZCD_STATUS	
3	**RG_VBIRX_ZCD_HYS_ENB**	RG_VBIRX_ZCD_HYS_ENB	**Enables voice buffer zero-detection hysteresis** 0: Enable 1: Disable
2:1	**RG_VBIRX_ZCD_CALI**	RG_VBIRX_ZCD_CALI	**Trims hysterisis of ZDTC** 00: 13mV 01: 26mV 10: 40mV

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Bit(s)	Mnemonic	Name	Description
			11: 56mV
0	**RG_VBIRX_ZCD_EN**	RG_VBIRX_ZCD_EN	**Enables VBIRX zero detection** 0: Disable 1: Enable

0714 **AUXADC_ADC0** **AUXADC ADC Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_ADC_RDY_BATSNS**	**RG_ADC_OUT_BATSNS**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_BATSNS**	RG_ADC_RDY_BATSNS	**AUXADC channel 0 output data ready for BATSNS** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_BATSNS**	RG_ADC_OUT_BATSNS	**AUXADC channel 0 output data for BATSNS**

0716 **AUXADC_ADC1** **AUXADC ADC Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_ADC_RDY_ISENSE**	**RG_ADC_OUT_ISENSE**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_ISENSE**	RG_ADC_RDY_ISENSE	**AUXADC channel 0 output data ready for ISENSE** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_ISENSE**	RG_ADC_OUT_ISENSE	**AUXADC channel 0 output data for ISENSE**

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0718 **AUXADC_ADC2** **AUXADC ADC Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_VCDT	RG_ADC_OUT_VCDT														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_VCDT**	RG_ADC_RDY_VCDT	**AUXADC channel 2 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_VCDT**	RG_ADC_OUT_VCDT	**AUXADC channel 2 output data**

071A **AUXADC_ADC3** **AUXADC ADC Register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_BATON1	RG_ADC_OUT_BATON1														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_BATON1**	RG_ADC_RDY_BATON1	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_BATON1**	RG_ADC_OUT_BATON1	**AUXADC channel 3 output data**

071C **AUXADC_ADC4** **AUXADC ADC Register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_TH	RG_ADC_OUT_THR_SENSE1														

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	R_SENSE1															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_THR_SENSE1**	RG_ADC_RDY_THR_SENSE1	**AUXADC channel 4 output data ready for THR_SENSE1** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_THR_SENSE1**	RG_ADC_OUT_THR_SENSE1	**AUXADC channel 4 output data for THR_SENSE1**

071E **AUXADC_ADC5** **AUXADC ADC Register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_THR_SENSE2	RG_ADC_OUT_THR_SENSE2														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_THR_SENSE2**	RG_ADC_RDY_THR_SENSE2	**AUXADC channel 4 output data ready for THR_SENSE2** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_THR_SENSE2**	RG_ADC_OUT_THR_SENSE2	**AUXADC channel 4 output data for THR_SENSE2**

0720 **AUXADC_ADC6** **AUXADC ADC Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_BATON2	RG_ADC_OUT_BATON2														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_BATON2**	RG_ADC_RDY_BATON2	**AUXADC channel 3 output data ready for BATON2** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_BATON2**	RG_ADC_OUT_BATON2	**AUXADC channel 3 output data for BATON2**

0722 **AUXADC_ADC7** **AUXADC ADC Register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_CH5	RG_ADC_OUT_CH5														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_CH5**	RG_ADC_RDY_CH5	**AUXADC channel 5 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_CH5**	RG_ADC_OUT_CH5	**AUXADC channel 5 output data**

0724 **AUXADC_ADC8** **AUXADC ADC Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_WAKEUP_PCHR	RG_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_WAKEUP_PCHR**	RG_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup PCHR output data ready** 0: AUXADC wakeup PCHR data not ready 1: AUXADC wakeup PCHR data ready
14:0	**RG_ADC_OUT_WAKEUP_PC**	RG_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup PCHR output data**

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Bit(s)	Mnemonic	Name	Description
	HR		

0726 **AUXADC_ADC9** **AUXADC ADC Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_ADC_RDY_WAKEUP_SWCHR**	**RG_ADC_OUT_WAKEUP_SWCHR**														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_WAKEUP_SWCHR**	RG_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup SWCHR output data ready** 0: AUXADC wakeup SWCHR data not ready 1: AUXADC wakeup SWCHR data ready
14:0	**RG_ADC_OUT_WAKEUP_SWCHR**	RG_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup SWCHR output data**

0728 **AUXADC_ADC10** **AUXADC ADC Register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RG_ADC_RDY_LBAT**				**RG_ADC_OUT_LBAT**											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_LBAT**	RG_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC low battery data proceeding 1: AUXADC low battery data ready
11:0	**RG_ADC_OUT_LBAT**	RG_ADC_OUT_LBAT	**AUXADC low battery output data**

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072A AUXADC_ADC11 AUXADC ADC Register 11 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_CH6	RG_ADC_OUT_CH6														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_CH6**	RG_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	**RG_ADC_OUT_CH6**	RG_ADC_OUT_CH6	**AUXADC channel 6 output data**

072C AUXADC_ADC12 AUXADC ADC Register 12 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_RDY_GPS															
Type	RO															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15	**RG_ADC_RDY_GPS**	RG_ADC_RDY_GPS	**AUXADC channel 7 output data ready for GPS** 0: AUXADC data proceeding 1: AUXADC data ready

072E AUXADC_ADC13 AUXADC ADC Register 13 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_OUT_GPS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_ADC_OUT_GPS**	RG_ADC_OUT_GPS	AUXADC channel 7 output data for GPS

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0730	AUXADC_ADC14	AUXADC ADC Register 14	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_OUT_GPS_LSB															
Type	RO															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15	RG_ADC_OUT_GPS_LSB	RG_ADC_OUT_GPS_LSB	AUXADC channel 7 output data for GPS LSB

0732	AUXADC_ADC15	AUXADC ADC Register 15	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_OUT_MD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_ADC_OUT_MD	RG_ADC_OUT_MD	AUXADC channel 7 output data for MD

0738	AUXADC_ADC18	AUXADC ADC Register 18	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_OUT_CIC_RAW_16_1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	RG_ADC_OUT_CIC_RAW_16_1	RG_ADC_OUT_CIC_RAW_16_1	cic raw data[16:1]

073A	AUXADC_ADC19	AUXADC ADC Register 19	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_BUSY															RG_A

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		DC_OUT_CIC_RAW_0
Type	RO	RO

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:1	**RG_ADC_BUSY**	RG_ADC_BUSY	15{adc_busy}, cic raw data[0]
0	**RG_ADC_OUT_CIC_RAW_0**	RG_ADC_OUT_CIC_RAW_0	15{adc_busy}, cic raw data[0]

073C [AUXADC_ADC20] AUXADC ADC Register 20 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_ADC_OUT_RSV3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**RG_ADC_OUT_RSV3**	RG_ADC_OUT_RSV3	

074E [AUXADC_CON6] AUXADC Control Register 6 8000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_LBAT_VOLT_MIN											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11:0	**RG_LBAT_VOLT_MIN**	RG_LBAT_VOLT_MIN	Low battery detection voltage

Module name: abbafe_top Base address: (+0h)

Address	Name	Width	Register function
0000	**ABB_AFE_CON0**	16	ABBAFE Top Enable
0002	**ABB_AFE_CON1**	16	ABBAFE Top Controls
0004	**ABB_AFE_CON2**	16	ABBAFE Top Muxs

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Address	Name	Width	Register function
0006	ABB_AFE_CON3	16	ABBAFE L-ch DC Compensation Value
0008	ABB_AFE_CON4	16	ABBAFE R-ch DC Compensation Value
0010	ABB_AFE_CON8	16	ABBAFE Sine Table Controls
0012	ABB_AFE_CON9	16	ABBAFE Digital MIC Controls
0014	ABB_AFE_CON10	16	ABBAFE DC Controls
0016	ABB_AFE_CON11	16	ABBAFE Inverse Enable Status
0018	ABB_AFE_STA0	16	ABBAFE Status Register 0
001A	ABB_AFE_STA1	16	ABBAFE Status Register 1
001C	ABB_AFE_STA2	16	ABBAFE Status Register 2
002C	AFE_TOP_CON0	16	**AFE Top Control Register 0** Control register for loopback test
002E	AFE_MON_DEBUG0	16	AFE Test Monitor Output

0000 **ABB_AFE_CON0** **ABBAFE Top Enable** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															ul_en	dl_en
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1		ul_en	**Enables Uplink turn-on** Squence: 1. Read abbafe inverse stable register [0]. 2. Write this register. 3. Write inverse bit at inverse stable register[8].
0		dl_en	**Enables downlink turn-on** Sequence: 1. Read abbafe inverse stable register [0]. 2. Write this register. 3. Write inverse bit at inverse stable register[8].

0002 **ABB_AFE_CON1** **ABBAFE Top Controls** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												ul_rate	dl_rate			
Type												RW	RW			
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		ul_rate	**Uplink SRC rate** 1'b0: SRC to 64K

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Bit(s)	Mnemonic	Name	Description
			1'b1: SRC to 96K Sequence: 1. Read abbafe inverse stable register [0]. 2. Write this register. 3. Write inverse bit at inverse stable register[8].
3:0		dl_rate	**DL 8X data rate** 4'd0: 8K X 8 4'd1: 11.025K X 8 4'd2: 12K X 8 4'd4: 16K X 8 4'd5: 22.05K X 8 4'd6: 24K X 8 4'd8: 32K X 8 4'd9: 44.1K X 8 4'd10: 48K X 8 Sequence: 1. Read abbafe inverse stable register [0]. 2. Write this register. 3. Write inverse bit at inverse stable register[8].

0004 **ABB_AFE_CON2** **ABBAFE Top Muxs** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					lch_mute	rch_mute		ul_lr_swap	dl_lr_swap	dl_r_eq_l	dl_l_inv	dl_tst_mux0	dl_ul_lpbk	ul_sine_on	dl_sine_on	ul_dl_lpbk
Type					RW	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0		0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
11		lch_mute	Disables l channel output
10		rch_mute	Disables r channel output
8		ul_lr_swap	Swaps uplink analog mic LR data
7		dl_lr_swap	Swaps downlink LR data
6		dl_r_eq_l	Downlink R-ch data = L-ch data
5		dl_l_inv	Inverts downlink L-ch data
4		dl_tst_mux0	**Downlink test mode mux0** Data from A_func_din
3		dl_ul_lpbk	Loops back downlink data to uplink
2		ul_sine_on	Sine table output mux to ABBAFE uplink output
1		dl_sine_on	Sine table output mux to ABBAFE downlink input
0		ul_dl_lpbk	Loops back uplink data to downlink

0006 **ABB_AFE_CON3** **ABBAFE L-ch DC Compensation Value** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lch_dccomp_val															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		lch_dccomp_val	L-ch DC compensation value. S0.15

0008 ABB_AFE_CON4 ABBAFE R-ch DC Compensation Value 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rch_dccomp_val															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		rch_dccomp_val	R-ch DC compensation value. S0.15

0010 ABB_AFE_CON8 ABBAFE Sine Table Controls 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sine_on	sine_mode		sine_dl_en	sine_freq								sine_amp			
Type	RW	RW		RW	RW								RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		sine_on	**Enables SINE table**
14:13		sine_mode	**Selects SINE table mode** 2'h0: Sine output 2'h1: Zero output
12		sine_dl_en	**SINE table base rate depends on downlink or uplink**
11:4		sine_freq	**Frequency setting of SRC sine table** Frequency = Sampling rate/64*FREQ_DIV
3:0		sine_amp	**SINE table amplitude** Amp = Full scale*(1/2)^SINE_AMP

0012 ABB_AFE_CON9 ABBAFE Digital MIC Controls 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	lch_phase			rch_phase			ck_phase	two_wire_en				dig_mic_en				d3p25m_sel
Type	RW			RW			RW	RW				RW				RW
Reset	0	0	0	0	0	0	0	0				0				0

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Bit(s)	Mnemonic	Name	Description
15:13		lch_phase	**DMIC l-ch phase**
12:10		rch_phase	**DMIC r-ch phase**
9		ck_phase	**DMIC clock phase**
8		two_wire_en	0: One-wire 1: Two-wire
4		dig_mic_en	0: Enable analog mic 1: Enable digital mic
0		d3p25m_sel	0: 1.625M sample rate 1: 3.25M sample rate

0014 **ABB_AFE_CON10** **ABBAFE DC Controls** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**dccomp_en**
Type																RW
Reset																1

Bit(s)	Mnemonic	Name	Description
0		dccomp_en	**Enables DC compensation** Sequence: 1. Read abbafe inverse stable register [1]. 2. Write this register. 3. Write inverse bit at inverse stable register[9].

0016 **ABB_AFE_CON11** **ABBAFE Inverse Enable Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**dc_status**	**top_ctrl_status**							**dc_status_now**	**top_ctrl_status_now**
Type							RW	RW							RO	RO
Reset							0	0							0	0

Bit(s)	Mnemonic	Name	Description
9		dc_status	Inverse current bit to update DC value and DC controls
8		top_ctrl_status	Inverse current bit to update ABBAFE top control register values
1		dc_status_now	Current DC status
0		top_ctrl_status_now	Current top ctrl status

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0018 **ABB_AFE_STA0** **ABBAFE Status Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										dl_en_sta	ul_en_sta	ul_rate_sta	dl_rate_sta			
Type										RO	RO	RO	RO			
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		dl_en_sta	Current downlink status
5		ul_en_sta	Current uplink status
4		ul_rate_sta	Current uplink rate status
3:0		dl_rate_sta	Current downlink rate status

001A **ABB_AFE_STA1** **ABBAFE Status Register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cur_lch_dc_val															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		cur_lch_dc_val	Current L-ch DC value

001C **ABB_AFE_STA2** **ABBAFE Status Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	cur_rch_dc_val															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0		cur_rch_dc_val	Current R-ch DC value

002C **AFE_TOP_CON0** **AFE Top Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	loopback_test2	loopback_test1														
Type	RW	RW														
Reset	0	0														

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Bit(s)	Mnemonic	Name	Description
15		loopback_test2	**Built-in loop-back test mode for up8x_txif_adc sources from 0 (analog input path) or from 1 (AP side)** 0: up8x_txif_adc normal path from cic input path 1: up8x_txif_adc loopback path from up8x_rxif (dac newif), i.e. sources from AP side.
14		loopback_test1	**Built-in loop-back test mode for up8x_rxif sources from 0 (normal input path from AP side) or from 1 (testing path from PMIC ADC side)** 0: up8x_rxif normal path from AP side 1: up8x_rxif loopback path from up8x_txif_adc (adc newif), i.e. sources from pmic adc side.

002E **AFE_MON_DEBUG0** **AFE Test Monitor Output** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													audio_sys_top_mon_sel			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		audio_sys_top_mon_sel	Selects FT audio_sys_top monitor debugging output

8000 **RTC_BBPU** **Baseband power up** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	KEY_BBPU									CBUSY	RELOAD	CLRPKY	AUTO	BBPU		PWREN
Type	WO									RO	WO	WO	RW	RW		RW
Reset	0	0	0	0	0	0	0	0		0	0	0	0	0		0

Overview

Bit(s)	Mnemonic	Name	Description
15:8	KEY_BBPU	KEY_BBPU	**A bus write is acceptable only when KEY_BBPU=0x43.**
6	CBUSY	CBUSY	**The read/write channels between RTC / Core is busy. This bit indicates high after software program sequence to anyone of RTC data registers and enable the transfer by RTC_WRTGR=1. By the way, it is high after the reset from low to high because RTC reload process.**
5	RELOAD	RELOAD	**Reload the values from RTC domain to Core domain. Generally speaking, RTC will reload synchronize the data from RTC to core when reset from 0 to 1. This bit can be treated as debug bit.**
4	CLRPKY	CLRPKY	**Clear powerkey1 and powerkey2 at the same time. In some cases, software may clear powerkey1 & powerkey2. The BBWAKEUP depends on the matching specific patterns of powerkey1 and powerkey2. If any one of powerkey1 or powerkey2 or BBPU is cleared, BBWAKEUP goes low immediately. Software can't program the other control bits without power. By program RTC_BBPU with CLRPKY=1 and BBPU=0 condition, RTC can clear powerkey1, powerkey2 and BBPU at the same moment.**

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3	**AUTO**	AUTO	**Controls if BBWAKEUP is automatically in the low state when SYSRST# transitions from high to low.** 0: BBWAKEUP is not automatically in the low state when SYSRST# transitions from high to low. 1: BBWAKEUP is automatically in the low state when SYSRST# transitions from high to low. The function is only active when RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values.
2	**BBPU**	BBPU	**Controls the power of PMIC. If powerkey1=A357h and powerkey2=67D2h, PMIC takes on the value programmed by software; otherwise PMIC is low.** 0: Power down 1: Power on
0	**PWREN**	PWREN	0: RTC alarm has no action on power switch. 1: When an RTC alarm occurs, BBPU is set to 1 and the system powers on by RTC alarm wakeup.

8002 RTC_IRQ_STA RTC IRQ status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne													LPSTA		TCSTA	ALSTA
Type													RO		RC	RC
Reset													0		0	0

Overview **This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.**

Bit(s)	Mnemonic	Name	Description
3	**LPSTA**	LPSTA	**This register indicates the IRQ status and whether or not the LPD asserts.** 0: No IRQ occurred; the 32K clock is good. 1: IRQ occurred; the 32K clock stopped or stops. This can be masked by LP_EN or cleared by initialize LPD.
1	**TCSTA**	TCSTA	**This register indicates the IRQ status and whether or not the tick condition has been met.** 0: No IRQ occurred; the tick condition has not been met. 1: IRQ occurred; the tick condition has been met.
0	**ALSTA**	ALSTA	**This register indicates the IRQ status and whether or not the alarm condition has been met.** 0: No IRQ occurred; the alarm condition has not been met. 1: IRQ occurred; the alarm condition has been met.

8004 RTC_IRQ_EN RTC IRQ enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne													LP_EN	ONESHOT	TC_EN	AL_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Overview **This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.**

Bit(s)	Mnemonic	Name	Description
3	**LP_EN**	LP_EN	**This register enables the control bit for IRQ generation if the Low power**

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Bit(s)	Mnemonic	Name	Description
			detected (32k clock off). 0: Disable IRQ generations. 1: Enable the LPD.
2	ONESHOT	ONESHOT	**Controls automatic reset of AL_EN and TC_EN.**
1	TC_EN	TC_EN	**This register enables the control bit for IRQ generation if the tick condition has been met.** 0: Disable IRQ generations. 1: Enable the tick time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.
0	AL_EN	AL_EN	**This register enables the control bit for IRQ generation if the alarm condition has been met.** 0: Disable IRQ generations. 1: Enable the alarm time match interrupt. Clear the interrupt when ONESHOT is high upon generation of the corresponding IRQ.

8006 RTC_CII_EN Counter increment IRQ enable 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne							1/8SECCII	1/4SECCII	1/2SECCII	YEACII	MTHCII	DOWCII	DOMCII	HOUCII	MINCII	SECCII
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Overview **This register activates or de-activates the IRQ generation when the TC counter reaches its maximum value.**

Bit(s)	Mnemonic	Name	Description
9	1/8SECCII	SECCII_1_8	**Set the bit to 1 to activate the IRQ at each one-eighth of a second update.**
8	1/4SECCII	SECCII_1_4	**Set the bit to 1 to activate the IRQ at each one-fourth of a second update.**
7	1/2SECCII	SECCII_1_2	**Set the bit to 1 to activate the IRQ at each one-half of a second update.**
6	YEACII	YEACII	**Set the bit to 1 to activate the IRQ at each year update.**
5	MTHCII	MTHCII	**Set the bit to 1 to activate the IRQ at each month update.**
4	DOWCII	DOWCII	**Set the bit to 1 to activate the IRQ at each day-of-week update.**
3	DOMCII	DOMCII	**Set the bit to 1 to activate the IRQ at each day-of-month update.**
2	HOUCII	HOUCII	**Set the bit to 1 to activate the IRQ at each hour update.**
1	MINCII	MINCII	**Set the bit to 1 to activate the IRQ at each minute update.**
0	SECCII	SECCII	**Set this bit to 1 to activate the IRQ at each second update.**

8008 RTC_AL_MASK RTC alarm mask 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne										YEA_MSK	MTH_MSK	DOW_MSK	DOM_MSK	HOU_MSK	MIN_MSK	SEC_MSK
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Overview **The alarm condition for alarm IRQ generation depends on whether or not the corresponding bit in**

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this register is masked. Warning: If you set all bits 1 in RTC_AL_MASK (i.e. RTC_AL_MASK=0x7f) and PWREN=1 in RTC_BBPU, it means alarm comes EVERY SECOND, not disabled.

Bit(s)	Mnemonic	Name	Description
6	**YEA_MSK**	YEA_MSK	0: Condition (RTC_TC_YEA = RTC_AL_YEA) is checked to generate the alarm signal. 1: Condition (RTC_TC_YEA = RTC_AL_YEA) is masked, i.e. the value of RTC_TC_YEA does not affect the alarm IRQ generation.
5	**MTH_MSK**	MTH_MSK	0: Condition (RTC_TC_MTH = RTC_AL_MTH) is checked to generate the alarm signal. 1: Condition (RTC_TC_MTH = RTC_AL_MTH) is masked, i.e. the value of RTC_TC_MTH does not affect the alarm IRQ generation.
4	**DOW_MSK**	DOW_MSK	0: Condition (RTC_TC_DOW = RTC_AL_DOW) is checked to generate the alarm signal. 1: Condition (RTC_TC_DOW = RTC_AL_DOW) is masked, i.e. the value of RTC_TC_DOW does not affect the alarm IRQ generation.
3	**DOM_MSK**	DOM_MSK	0: Condition (RTC_TC_DOM = RTC_AL_DOM) is checked to generate the alarm signal. 1: Condition (RTC_TC_DOM = RTC_AL_DOM) is masked, i.e. the value of RTC_TC_DOM does not affect the alarm IRQ generation.
2	**HOU_MSK**	HOU_MSK	0: Condition (RTC_TC_HOU = RTC_AL_HOU) is checked to generate the alarm signal. 1: Condition (RTC_TC_HOU = RTC_AL_HOU) is masked, i.e. the value of RTC_TC_HOU does not affect the alarm IRQ generation.
1	**MIN_MSK**	MIN_MSK	0: Condition (RTC_TC_MIN = RTC_AL_MIN) is checked to generate the alarm signal. 1: Condition (RTC_TC_MIN = RTC_AL_MIN) is masked, i.e. the value of RTC_TC_MIN does not affect the alarm IRQ generation.
0	**SEC_MSK**	SEC_MSK	0: Condition (RTC_TC_SEC = RTC_AL_SEC) is checked to generate the alarm signal. 1: Condition (RTC_TC_SEC = RTC_AL_SEC) is masked, i.e. the value of RTC_TC_SEC does not affect the alarm IRQ generation.

800A RTC_TC_SEC RTC seconds time counter register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne											TC_SECOND					
Type											RW					
Reset											0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
5:0	**TC_SECOND**	TC_SECOND	**The second initial value for the time counter. The range of its value is: 0-59.**

800C RTC_TC_MIN RTC minutes time counter register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne											TC_MINUTE					
Type											RW					
Reset											0	0	0	0	0	0

Overview

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Bit(s)	Mnemonic	Name	Description
5:0	TC_MINUTE	TC_MINUTE	The minute initial value for the time counter. The range of its value is: 0-59.

800E RTC_TC_HOU RTC hours time counter register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne												TC_HOUR				
Type												RW				
Reset												0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
4:0	TC_HOUR	TC_HOUR	The hour initial value for the time counter. The range of its value is: 0-23.

8010 RTC_TC_DOM RTC day-of-month time counter register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne												TC_DOM				
Type												RW				
Reset												0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
4:0	TC_DOM	TC_DOM	The day-of-month initial value for the time counter. The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

8012 RTC_TC_DOW RTC day-of-week time counter register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne														TC_DOW		
Type														RW		
Reset														0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
2:0	TC_DOW	TC_DOW	The day-of-week initial value for the time counter. The range of its value is: 1-7.

8014 RTC_TC_MTH RTC month time counter register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne													TC_MONTH			

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Type													RW			
Reset													0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
3:0	TC_MONTH	TC_MONTH	**The month initial value for the time counter. The range of its value is: 1-12.**

8016 RTC_TC_YEA RTC year time counter register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne										TC_YEAR						
Type										RW						
Reset										0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
6:0	TC_YEAR	TC_YEAR	**The year initial value for the time counter. The range of its value is: 0-127. (2000-2127).** Software can bias the year as multiples of 4 for the internal leap-year formula. Here are 3 examples: 2000-2127, 1972~2099, 1904~2031.To simplify, RTC hardware treats all 4-multiple as leap years. If the range you defined includes non-leap 4-multiple year (say: 2100), you have to adjust to correct date by yourselves. (ex: change Feb. 29th, 2100 to Mar. 1st, 2100). It's suggested to bias the range large than 1900 and less then 2100 to evade the manual adjusting. I.e.: the bias values are suggested to be in the range of [-28,-96], that are (1972~ 2099) ~ (1904~ 2031). The formal leap formula: if year modulo 400 is 0 then leap else if year modulo 100 is 0 then no_leap else if year modulo 4 is 0 then leap else no_leap

8018 RTC_AL_SEC RTC second alarm setting register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne											AL_SECOND					
Type											RW					
Reset											0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
5:0	AL_SECOND	AL_SECOND	**The second value of the alarm counter setting. The range of its value is: 0-59.**

801A RTC_AL_MIN RTC minute alarm setting register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne											AL_MINUTE					

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Type											RW					
Reset											0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
5:0	AL_MINUTE	AL_MINUTE	The minute value of the alarm counter setting. The range of its value is: 0-59.

801C RTC_AL_HOU RTC hour alarm setting register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	NEW_SPARE0											AL_HOUR				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
15:8		NEW_SPARE0	The registers are reserved for specific purposes.
4:0	AL_HOUR	AL_HOUR	The hour value of the alarm counter setting. The range of its value is: 0-23.

801E RTC_AL_DOM RTC day-of-month alarm setting register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	NEW_SPARE1											AL_DOM				
Type	RW											RW				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
15:8		NEW_SPARE1	The registers are reserved for specific purposes.
4:0	AL_DOM	AL_DOM	The day-of-month value of the alarm counter setting. The day-of-month maximum value depends on the leap year condition, i.e. 2 LSB of year time counter are zeros.

8020 RTC_AL_DOW RTC day-of-week alarm setting register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	NEW_SPARE2													AL_DOW		
Type	RW													RW		
Reset	0	0	0	0	0	0	0	0						0	0	0

Overview

Bit(s)	Mnemonic	Name	Description

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15:8		NEW_SPARE2	**The registers are reserved for specific purposes.**
2:0	**AL_DOW**	AL_DOW	**The day-of-week value of the alarm counter setting. The range of its value is: 1-7.**

8022 RTC_AL_MTH RTC month alarm setting register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	NEW_SPARE3												AL_MONTH			
Type	RW												RW			
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
15:8		NEW_SPARE3	**The registers are reserved for specific purposes.**
3:0	**AL_MONTH**	AL_MONTH	**The month value of the alarm counter setting. The range of its value is: 1-12.**

8024 RTC_AL_YEA RTC year alarm setting register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne										AL_YEAR						
Type										RW						
Reset										0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
6:0	**AL_YEAR**	AL_YEAR	**The year value of the alarm counter setting. The range of its value is: 0-127. (2000-2127)**

8026 RTC_OSC32CON OSC32 control 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	XOSC_FTUNE		LNBUF_CALI	LNBUF_EN	AMP_GSEL	AMPCTL_EN	RTC_OSC32_OPT		RTC_EMBCK_SEL	RTC_EMBCK_SEL_MODE	RTC_XOSC32_ENB	XOSCCALI				
Type	WO		WO	RW	RW	RW	RW		RO	RW	RO	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview **The function is only active when RTC_POWERKEY1 & RTC_POWERKEY2 match the correct values. When powerkeys do not match, the internal xosccali=0x7.**

Bit(s)	Mnemonic	Name	Description
15:14	**XOSC_FTU**	RTC_OSC32_RSV	**RSV**

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	NE		
13	LNBUF_CALI	RTC_REG_XOSC32_ENB	**XOSC32_ENB = 0 (32k crystal exist)** XOSC32_ENB = 1 (32k crystal doesn't exist)
12	LNBUF_EN	RTC_OSC32_RSV	**RSV**
11	AMP_GSEL	RTC_EMBCK_SEL_OPTION	**0: embedded clock switch back to dcxo decided by (oesc32_ck_alive & powerkey_match)** 1: embedded clock switch back to dcxo decided by (powerkey_match)
10	AMPCTL_EN	RTC_OSC32_RSV	**RSV**
9:8	RTC_OSC32_OPT	RTC_OSC32_RSV	**RSV**
7		RTC_EMBCK_SEL	**0: dcxo_ck** 1: eosc32_ck
6		RTC_EMBCK_SEL_MODE	**0: embedded clock hw auto select** 1: embedded clock sw control mode
5		RTC_XOSC32_ENB	**XOSC32_ENB = 0 (32k crystal exist)** XOSC32_ENB = 1 (32k crystal doesn't exist)
4:0	XOSCCALI	XOSCCALI	**GM calibration** Default 4'b0111, 2nd step suggest to set to 4'b0000 EOSC_CALI = charging cap calibration

The OSC32CON is not protected by RTC_PROT because RTC_PROT needs 32.768KHz clock to unlock. Similarly, to modify RTC_OSC32CON does not need to write RTC_WRTGR neither. To protect the osc32 control bits, you have to follow the update sequence to update RTC_OSC32CON. After you complete the updating sequence, you have to reload to get the internal RTC_OSC32CON.

Update sequence:

Step 1: Write RTC_OSC32CON = 0x1a57 and wait until CBUSY=0
Step 2: Write RTC_OSC32CON = 0x2b68 and wait until CBUSY=0
Step 3: Write the real value you want to write RTC_OSC32CON and wait until CBUSY=0
Step 4: Go to step 1 if you need to modify RTC_OSC32CON again.

8028 RTC_POWERKEY1 RTC_POWERKEY1 register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	RTC_POWERKEY1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

802A RTC_POWERKEY2 RTC_POWERKEY2 register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	RTC_POWERKEY2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

These register sets are used to determine if the real time clock has been programmed by software; i.e. the time value in real time clock is correct. When the real time clock is first powered on, the register contents are all undefined, therefore the time values shown are incorrect. Software needs to know if the real time clock has

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been programmed. Hence, these two registers are defined to solve this power-on issue. After software programs the correct value, these two register sets do not need to be updated. In addition to programming the correct time value, when the contents of these register sets are wrong, the interrupt is not generated. Therefore, the real time clock does not generate the interrupts before the software programs the registers; unwanted interrupt due to wrong time value do not occur. The correct values of these two register sets are:

RTC_POWERKEY1 A357h
RTC_POWERKEY2 67D2h

802C RTC_PDN1 PDN1 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	RTC_PDN1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
15:0	RTC_PDN1	RTC_PDN1	**The spare registers for software to keep power on and power off state information.**

802E RTC_PDN2 PDN2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	RTC_PDN2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
15:0	RTC_PDN2	RTC_PDN2	**The spare registers for software to keep power on and power off state information.**

8030 RTC_SPAR0 Spare register for specific purpose 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	RTC_SPAR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
15:0	RTC_SPAR0	RTC_SPAR0	**The registers are reserved for specific purposes.**

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8032 RTC_SPAR1 Spare register for specific purpose 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	RTC_SPAR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
15:0	RTC_SPAR1	RTC_SPAR1	**The registers are reserved for specific purposes.**

8036 RTC_PROT Lock/unlock scheme to prevent RTC miswriting 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	RTC_PROT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description

15:0	RTC_PROT	RTC_PROT	**The RTC write interface is protected by RTC_PROT. Whether the RTC writing interface is enabled or not is decided by RTC_PROT contents. When RTC_POWERKEY1 & RTC_POWERKEY2 are not equal to the correct values, the RTC writing interface is always enabled. But when they match, users have to perform Unlock flow to enable the writing interface.**
			
			Unlock flow:
			Step1: *RTC_PROT=0x586a;
			Step2: *RTC_WRTGR=1;
			Step3: while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec
			Step4: *RTC_PROT=0x9136;
			Step5: *RTC_WRTGR=1;
			Step6: while(*RTC_BBPU & 0x40) {}; // Timeout period: 120usec
			
			Notice: Please always keep RTC in unlock state in power on mode. Once the normal RTC content writing is complete, DO NOT modify the RTC_PROT content to lock RTC. The RTC_PROT contents will be clear automatically when power off immediately.

8038 RTC_DIFF One-time calibration offset 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne					RTC_DIFF											
Type					RW											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Overview **This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.**

Bit(s)	Mnemonic	Name	Description
11:0	RTC_DIFF	RTC_DIFF	**These registers are used to adjust the internal counter of RTC. It effects**

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		once and returns to zero in done. In some cases, you observe the RTC is faster or slower than the standard. To change RTC_TC_SEC is coarse and may cause alarm problem. RTC_DIFF provides a finer time unit. An internal 15-bit counter accumulates in each 32768-HZ clock. Entering a non-zero value into the RTC_DIFF causes the internal RTC counter increases or decreases RTC_DIFF when RTC_DIFF changes to zero again. RTC_DIFF represents as 2's completement form. For example, if you fill in 0xfff into RTC_DIFF, the internal counter decreases 1 when RTC_DIFF returns to zero. In other words, you can only use RTC_DIFF continuously if RTC_DIFF is equal to zero now. Note: RTC_DIFF ranges from 0x800 (-2048) to 0x7fd (2045). 0x7ff & 0x7fe are forbid to use.

803A RTC_CALI Repeat calibration offset 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne				BBPU_2SEC_STAT	BBPU_2SEC_STAT_CLEAR	BBPU_2SEC_MODE		BBPU_2SEC_EN		RTC_CALI						
Type				RO	RW	RW		RW		RW						
Reset				0	0	0	0	0		0	0	0	0	0	0	0

Overview **This register is fixed in 0 when RTC_POWERKEY1 & RTC_POWERKEY2 unmatch the correct values.**

Bit(s)	Mnemonic	Name	Description
12	BBPU_2SEC_STAT	BBPU_2SEC_STAT	**indicate if battery has been re-inserted within 2seconds**
11	BBPU_2SEC_STAT_CLEAR	BBPU_2SEC_STAT_CLEAR	**Clear Bbwakeup 2 sec event**
10:9	BBPU_2SEC_MODE	BBPU_2SEC_MODE	**2'b11: never powerdown** **2'b10: 2sec powerdown after battery is removed** **2'b01:1sec powerdown after battery is removed** **2'b01:0.5sec powerdown after battery is removed**
8	BBPU_2SEC_EN	BBPU_2SEC_EN	**0: legacy mode** 1: 2sec powerdown mode
6:0	RTC_CALI	RTC_CALI	**These registers provide a repeat calibration scheme. RTC_CALI provides 7-bit calibration capability in 8-second duration; in other words, 5-bit calibration capability in each second. RTC_CALI represents in 2's complement form, such that you can adjust RTC increasing or decreasing.** Due to RTC_CALI is revealed in 8 seconds, the resolution is less than a 1/32768 clock. Avg. resolution: 1/32768/8=3.81us Avg. adjust range: -0.244~0.240ms/sec in 2's complement: -0x40~0x3f (-64~63)

To disable this new feature, you need to set BBPU_2SEC_EN=0. Auto_powerdown bit can be used as before.

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803C RTC_WRTGR Enable the transfers from core to RTC in the queue 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne																WRTGR
Type																WO
Reset																0

Overview

Bit(s)	Mnemonic	Name	Description
0	WRTGR	WRTGR	**This register enables the transfers from core to RTC. After you modify all the RTC registers you'd like to change, you must write RTC_WRTGR to 1 to trigger the transfer. The prior writing operations are queued at core power domain. The pending data will not be transferred to RTC domain until WRTGR=1.** After WRTGR=1, the pending data is transferred to RTC domain sequentially in order of register address, from low to high. For example: RTC_BBPU -> RTC_IRQ_EN -> RTC_CII_EN -> RTC_AL_MASK -> RTC_TC_SEC -> etc. The CBUSY in RTC_BBPU is equal to 1 in writing process. You can observe CBUSY to determine when the transmission completes.

803E RTC_CON Other RTC control register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	LPSTA_RAW	GPI	GE8	GE4	GPU	GPEN	GSMT	GSR	GOE	GPO	F32KOB	CDBO	LPRST	LPEN		
Type	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Overview

Note: GPU,GOE,LPRST,LPEN are tie0 and GPEN,F32KOB are tie1 internally when RTC_POWERKEY1 & RTC_POWERKEY2 do not match the correct values. After changing the RTC_CON, you have to write WRTGR=1 to take effect.

Bit(s)	Mnemonic	Name	Description
15	LPSTA_RAW	LPSTA_RAW	**The raw status of LP_STA. You can re-initialize LPD to clear this bit. Notice: This bit is always high before LPD initialization sequence after the first power on.**
14	GPI	GPI	**The input value of RTC_GPIO when GOE=0. (input mode)**
13	GE8	GE8	**Driving capability of RTC_GPIO.**
12	GE4	GE4	**Driving capability of RTC_GPIO. See figure 1.**
11	GPU	GPU	**Pull-up of RTC_GPIO**
10	GPEN	GPEN	**Pull enable of RTC_GPIO. When GPEN=1, RTC_GPIO is pull up if GPU=1; pull down if GPU=0. See figure 2.**
9	GSMT	GSMT	**SMT of RTC_GPIO. Contr0l Pin for Smith Trigger Circuit.** 0: RTC_GPIO Smith Trigger off. 1: RTC_GPIO Smith Trigger on.
8	GSR	GSR	**SR of RTC_GPIO. Output Slew Rate Control. High asserted. SR=0, slower slew. SR=1.** 0: RTC_GPIO higher slew output. 1: RTC_GPIO slower slew output.
7	GOE	GOE	**OE of RTC_GPIO.** 0: RTC_GPIO is in input mode.

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			1: RTC_GPIO is in output mode.
6	GPO	GPO	**Output value of RTC_GPIO. Only active when GOE=1. (output mode)**
5	F32KOB	F32KOB	**Export 32.768KHz clock on RTC_GPIO.**
4	CDBO	CDBO	**Export COREDETB on RTC_GPIO. See figure 3.**
3	LPRST	LPRST	**To reset the LPDETB. This only takes effect when LPEN=1. When LPEN=0, the internal LPRST signal to XOSC32 is always 0.**
2	LPEN	LPEN	**To enable the LPDETB. The LP initialization sequence:** 1. write LPEN=1,LPRST=0. write RTC_WRTGR=1. wait cbusy down. 2. write LPEN=1,LPRST=1. write RTC_WRTGR=1. wait cbusy down. 3. write LPEN=1,LPRST=0. write RTC_WRTGR=1. wait cbusy down.

GE8	GE4	RTC_GPIO driving strength
0	0	4 mA
0	1	8 mA
1	0	12 mA
1	1	16 mA

Figure 4

GPEN	GPU	Function
0	X	No pull on RTC_GPIO
1	0	Pull down on RTC_GPIO
1	1	Pull up on RTC_GPIO

Figure 2

GOE	F32KOB	CDBO	GPO	Dir	Function
0	1	X	X	I	
X	0	X	X	O	Exports 32.768KHz clock
1	1	1	X	O	Exports COREDETB 0 : Vcore > 0.6V* 1 : Vcore < 0.6V* *The threshold voltage may change with process drift.
1	1	0	0	O	Exports 0 (ground)
1	1	0	1	O	Exports 1 (Vrtc)

Figure 3

When Vcore always exists, s/w can trust the registers and wait for LP interrupt from rtc if the 32.768KHz clock stopped or has been stopped.

But nothing is trusted after the battery OFF (Vrtc may drop). Every booting time, s/w has to check if the LPSTA_RAW=1. (LP_STA=LPSTA_RAW & LP_IRQ_EN) If true, then the RTC contents are no longer trusted just like powerkeys not match. You have to initialize RTC contents in this case.

Note: Always configure EMBCK_SEL in RTC_OSC32CON before configure GOE and F32KOB in RTC_CON.

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4 Application Notes

4.1 Hardware External Shutdown

The following schematic illustrates the hardware external shut-down function for MT6323L to power down when the main chip software crashes.

- Short press PWRKEY or FCHR_ENB
  - INT-> EINT -> software control
  - Power-down, sleep mode or the other functions
- Long press shut-down
  - Force power-off of PMU
  - 5/8/11/14 s with < 1% accuracy
  - External reset function with source from:
    - PWRKEY and FCHR_ENB both pressed for long period of time
      - PWRKEY and FCHR_ENB doesn’t use same key
    - PWERKEY pressed for long period of time
    - FCHR_ENB pressed for long period of time
      - Software disables watchdog counter
- Re-start
  - System will re-power on if keep long press PWRKEY after system shutdown

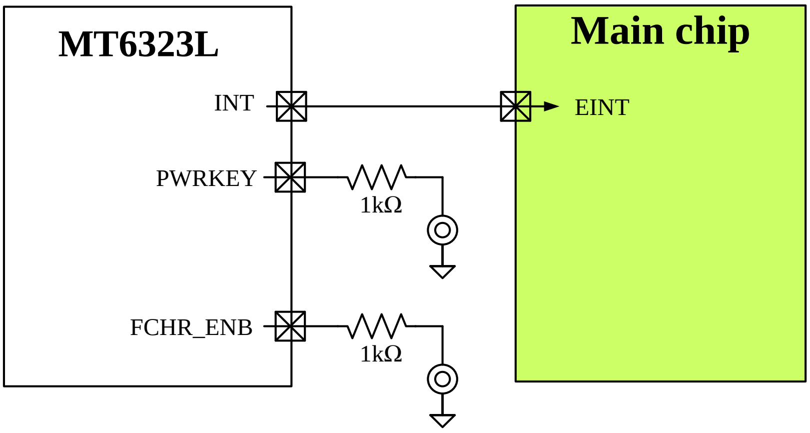

Figure 4-1. Hardware external shut-down function

4.2 Configuration for Unused Buck Converter

The figure below shows the configuration for MT6323L VPA buck converter that is not used .

- Configuration for VPA not in use:
  - VBAT_PA connect to VBAT; GND_PA connect to GND
  - VPA & VPA_FB: floating

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– RG_VPA_EN = 0 & RG_VPA_NDIS_EN = 1

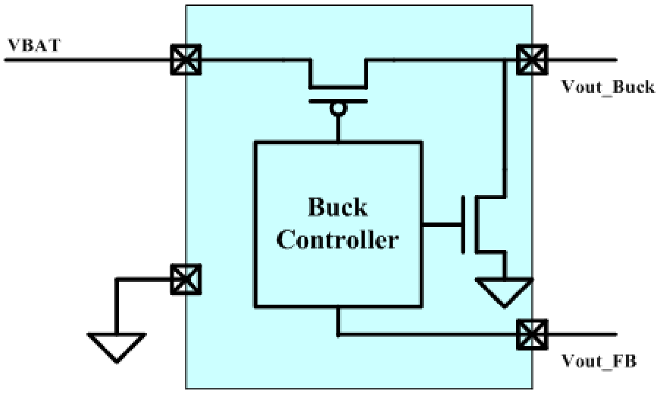

Figure 4-2. Configuration for unused DC/DC

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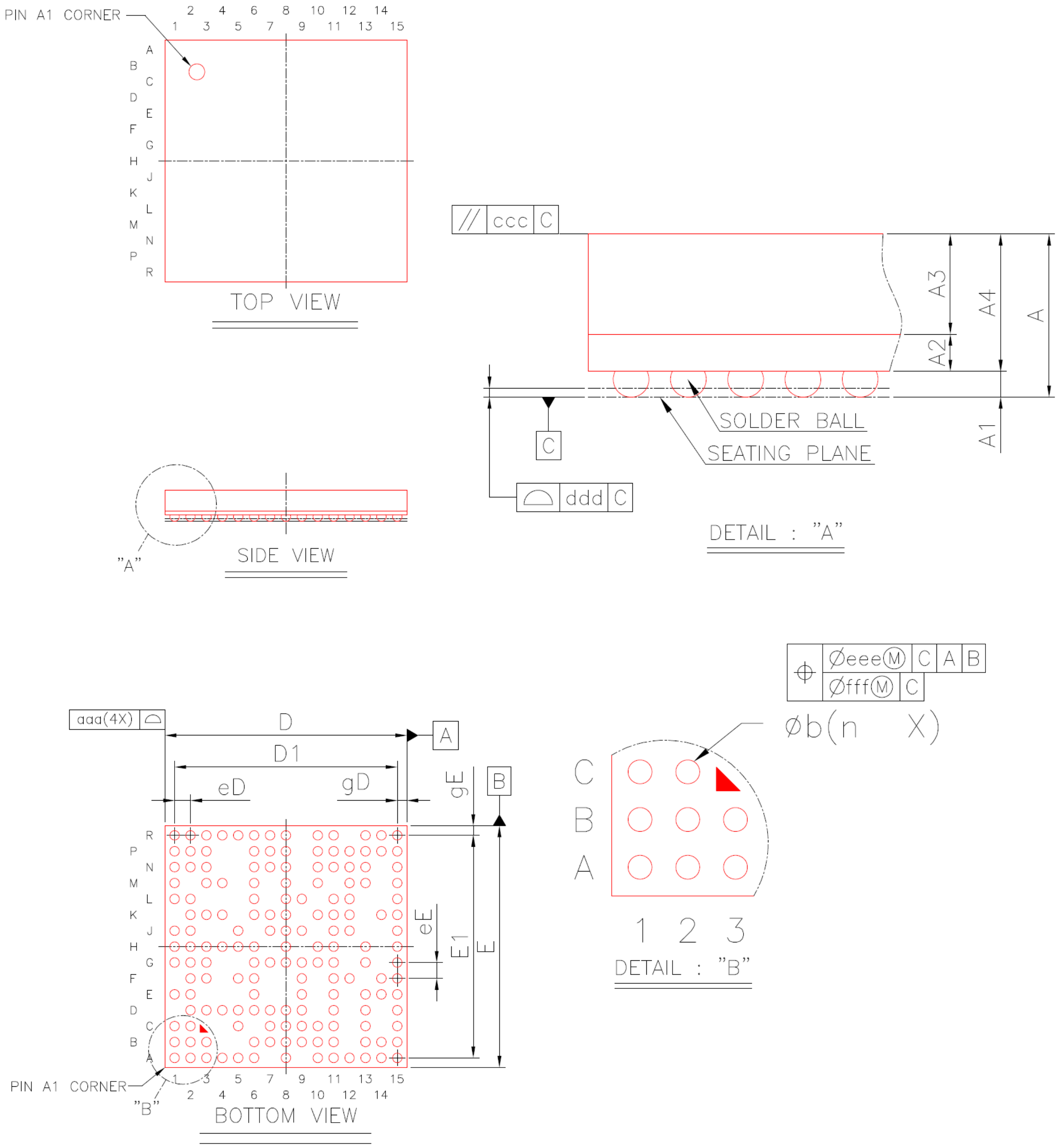
5 MT6323L Packaging

5.1 Package Dimensions



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Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	7.50	7.60	7.70
	Y	E	7.50	7.60	7.70
Ball Pitch	X	eD	0.50		
	Y	eE	0.50		
Mold Thickness		A3	0.65 Ref.		
Substrate Thickness		A2	0.11 Ref.		
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.05
Ball Diameter			0.30		
Ball Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa	0.10		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	158		
Edge Ball Center to Center	X	D1	7.00		
	Y	E1	7.00		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

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